SCALABLE SENSOR DATA PROCESSOR: A MULTI-CORE PAYLOAD DATA PROCESSOR ASIC

L. Berrojo[1], R. Moreno[1], R. Regada[1], E. García[1], R. Trautner[2], G. Rauwerda[3], K. Sunesen[3], Y. He[3], S. Redant[4], G. Thys[4], J. Andersson[5], S. Habinc[5]

[1]*Product Line Digital and Detection, Thales Alenia Space Spain (TAS-E), Einstein, 7 P.T.M., Tres Cantos, E-28760, Madrid, Spain, Tel. +34 918 077 900*
luis.berrojo@thalesaleniaspace.com

[2] *TEC-EDP, ESA/ESTEC*
P.O. Box 299, 2200AG Noordwijk, the Netherlands
Roland.Trautner@esa.int

[3]*Recore Systems BV*
P.O. Box 77, 7500 AB Enschede, The Netherlands
Gerard.Rauwerda@recoresystems.com

[4]*IMEC*
Kapeldreef 75,B-3001 Leuven,Belgium
steven.redant@imec.be

[5]*Cobham Gaisler*
Kungsgatan 12, SE-411 19 Göteborg, Sweden
sandi.habinc@gaisler.com

ABSTRACT

The Scalable Sensor Data Processor (SSDP) project, under ESA contract and with TAS-E as prime contractor, targets the development of a multi-core ASIC for payload data processing to be used, among other terrestrial and space application areas, in future scientific and exploration missions with harsh radiation environments. The SSDP is a mixed-signal heterogeneous multi-core System-on-Chip (SoC). It combines GPP and NoC-based DSP subsystems with on-chip ADCs and several standard space I/Fs to make a flexible, configurable and scalable device. The NoC comprises two state-of-the-art fixed point Xentium® DSP processors, providing the device with high data processing capabilities.

Keywords — Network On Chip, Digital Signal Processing, Mixed signal ASIC, Space Exploration, IP core.

1. INTRODUCTION

The need for processing power on board of spacecraft, and in particular for many types of payloads, is steadily increasing. Higher processing power allows doing more complex on-board pre-processing, data selection and compression, and allows reducing the requirements towards the space-Earth communication link by reducing the data volumes that need to be transmitted. In addition, increased processing power is also needed for specific applications such as optical navigation for exploration vehicles, where the reliable and fast processing of image data is the key to mission success.

At the same time, the desire for low mass, low power and low volume and radiation tolerance asks for higher integration of electronic functions. Recent technology developments such as mixed signal ASIC design libraries enable the integration of analog and digital components on a single chip, and allow the development of components that can replace what was implemented with a whole group of chips in previous designs.

Programmable processor ASICs provide key advantages in comparison to FPGAs w.r.t. operational flexibility and power consumption. In Europe, the SPARC based family of LEON general purpose processors is well established in space applications. Recent developments have led to the maturation of European Digital Signal Processor IP cores that form an ideal complement to GPPs for signal processing tasks due to their inherent parallelism and energy efficiency. The development of Network on Chip technology that allows connecting multiple GPP and DSP cores, bridges to fast interfaces and converters, and on-chip bus systems allow the design of high performance, scalable, and mixed signal ASICs with an unprecedented degree of integration.

2. THE SSDP PROJECT

The SSDP project is conceived to ensure the general availability of a new data processor with the highest degree of flexibility, configurability, connectivity, scalable processing power, high radiation tolerance, low power consumption, low

mass, and low volume to cover the needs of future missions including JUICE, and Lunar and Mars Landers.

JUICE [1] is a mission to the Jupiter system and its moons Callisto, Ganymede and Europa. Specific requirements of this mission include, in addition to the strong need for efficient power consumption and mass, high radiation tolerance (in the order of hundreds of krad) due to the specific challenges of the Jupiter system.

Lunar and Mars landers are foreseen to exploit optical navigation methods for controlled entry, descent and landing, creating a need for predictable high processing power combined with efficient interfaces to next generation imaging sensors, with low mass and low power consumption.

2.1. Objectives

The aim of the activity is to design, verify, manufacture, and validate a multi-core payload data processor SSDP ASIC. The SSDP processor is a mixed-signal SoC including 2 RECORE XENTIUM® VLIW Fixed Point DSP processors, a LEON3FT processor and associated peripherals for memory management and external data exchange. External data interfaces will be based in standard buses well established in the space industry such as SpaceWire, CAN, and SPI. The XENTIUM® subsystem will be connected by means of a RECORE proprietary high performance Network-on-Chip grid, while the LEON subsystem will be based in the traditional AMBA bus architecture. The subsystems will be interconnected by a NoC/AHB bridge. Analog parts will include fast instrumentation- and housekeeping ADCs, a 16 channel multiplexer, interfaces to temperature sensors, and a PLL.

The purpose of this multi-core processor is to manage the wealth of data collected in future space missions, coping with the stringent radiation requirements of missions such as JUICE [2]. The IMEC DARE 180 UMC platform has been selected for implementation due to its proven radiation performances, mixed signal capabilities, and the availability of required Analog IP blocks.

2.2. Consortium

In order to conduct the activities with an optimum and cost-effective effort, the established consortium includes IMEC, RECORE SYSTEMS, and ARQUIMEA; COBHAM GAISLER has been selected as the SSDP commercialization partner who will provide SSDP parts, related evaluation hardware and software as well as services to end users. TAS-E acts as prime of the activity; and is also in charge of the activities not covered by the subcontractors.

2.3. Heritage

The SSDP development will take advantage of previous projects like:

NGDSP: European DSP Trade-off & Definition Study: This activity included an assessment of MPPB and identified possible improvements.

LEONDARE, ASICs for Space Fabricated With Radiation Hardened by Design Library: This activity included evaluation and qualification of the DARE 180 UMC library with the LEON3FT processor and the GRFPU floating point unit.

Massively Parallel Processing Breadboard (MPPB)[3,4]*:* Early prototype with 2 Xentium® DSPs & 1 LEON2 GPP on a Xilinx FPGA, plus peripherals.

DARE+ Application ASIC: this activity improved and demonstrated the maturity of the DARE 180 UMC standard cell library for applications in radiation environments up to 1 Mrad TID [5].

NGAPP, Next Generation Astronomy Processing Platform: This activity included an evaluation of an MPPB and the SSDP preliminary specification for scientific astronomical missions.

2.4. SSDP architecture

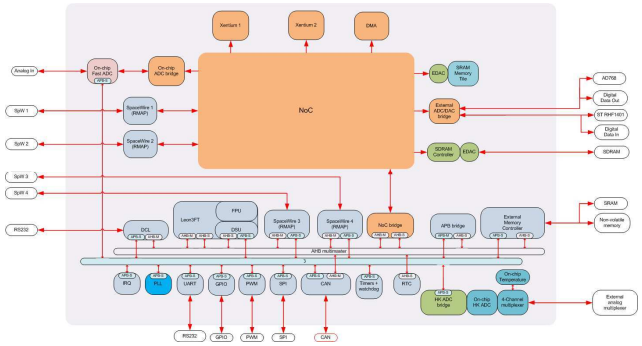

Figure 1: SSDP Architecture

As shown in ***Figure 1*** the SSDP is composed of 2 Xentium® DSPs (further detailed in section 2.5), connected by a NoC grid and the LEON subsystem connected by an AMBA bus.

The LEON subsystem is built around the LEON3FT COBHAM GAISLER processor IP.

The NoC-based DSP subsystem (***Figure 2***) is composed of the following blocks:

- 2 Xentium® processors running at 100 MHz.
- 1 DMA controller.
- 1 internal memory tile with a size of 64 KB.
- 1 ADC bridge, used for the internal fast ADC (provided by Arquimea) and for external ADC (from ICsense), and also as a digital parallel input port, that can be used for connection with additional SSDP devices.
- 1 External DAC bridge, used also as digital parallel output port, which can be used for connection with additional SSDP devices.

- 1 External SDRAM memory controller, with 32-bit access plus SEC/DED EDAC (40 bits in total).
- 2 SpW RMAP interfaces implemented as targets.
- The NoC itself: 32-bit packet-switched, 3.2 Gbps per link in each direction at 100 MHz system clock

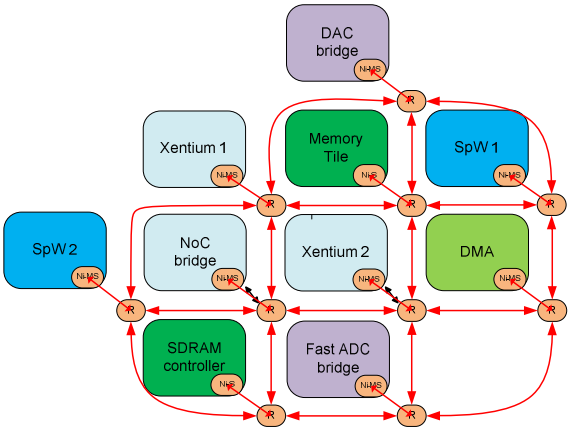

Figure 2: NoC Subsystem

2.5. Xentium

The Xentium® is a little-endian VLIW type processor developed by Recore Systems. The Xentium tile as depicted in ***Figure 2*** consists of three main parts: the Xentium local bus, the datapath (core) and the memory (bank 0 to 3). The Xentium® local bus is an AHB implementation to allow the use of already existing IP when needed. The datapath comprises ten parallel execution units including support for 40-bit accumulator, 32-bit word, 16-bit half-word, 8-bit byte, and 2-element 16-bit per element vector data types. The execution units combine to perform:

- 4 16-bit MACs/cycle, or
- 2 16-bit complex MACs/cycle, or
- 2 32-bit MACs/cycle.
- 4 32-bit load/store operations/cycle

The memory provides concurrent access to 4 different banks. This allows the datapath to load and/or store four 32-bit values simultaneously. This bandwidth is needed to make use of all different parallel execution units in the Xentium.

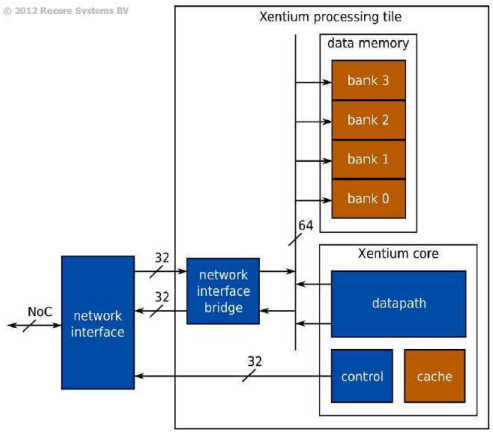

Figure 3: Xentium tile

2.6. Control flow

The running software is controlled by the GPP (i.e.: the LEON3FT) processor:

- All peripherals, including those on the NoC, are memory mapped to the LEON3FT.
- The communication is based on interrupts to the LEON3FT processor that distributes tasks accordingly.
- The Xentium® cores are used as accelerators, executing small data processing routines (aka kernels).

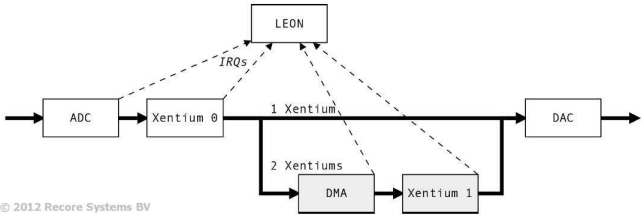

Figure 4: Example of control flow

2.7. Benchmarks

Functions representing typical operations in science, earth observation and communications data processing will be generated. Examples of these functions in previous MPPB related activities will be taken as reference and adapted to the new ASIC. Benchmarking will characterize I/O and performance capabilities including kernel and application benchmarks from the ESA Next Generation Space DSP SW Benchmarks [6]:

Kernel benchmarks: represent basic algorithms used in complex applications.

- Power-of-2 FFT.
- FIR filters.

Application benchmarks: reproduce domain-specific applications.

- CCSDS 121 RICE.
- CCSDS 122 image compression.

2.8. SSDP Improvements

Based on the completed assessments of MPPB in the NGDSP and NGAPP activities, and also based on an assessment performed by TAS-E, the following improvements will be implemented in the SSDP project with respect to MPPB:

- Addition of CAN interface
- Addition of SPI interface
- Addition of PWM output channels
- On-chip ADCs
- DMA transaction improvements
- EDAC memory protection
- SDE improvements
- Addition of on-target debugging hardware support
- Optimised DSP libraries
- Optimised Board Support Routines
- Inclusions of a GPP with a floating point unit (i.e. LEON3FT with GRFPU)

3. STATUS

At the date of presentation the project has reached the SRR milestone, with PDR, DDR and CDR following before Q1'2016. Prototypes are expected to be available in Q3'2016. A contract change for SSDP flight model development and evaluation / qualification is being implemented, and the acceptance review for the SSDP FMs is foreseen in Q2'2017. The ASIC commercialization will start in parallel.

4. CONCLUSION

Similar to other domains, spacecraft payload computers continuously require higher processing power, while at the same time low mass, small size and low power consumption are desired as well. Additionally, depending on the mission, also high radiation tolerance is often required. The Scalable Sensor Data Processor will provide a solution that covers all these requirements. We have presented the SSDP project, which includes the design, development and validation of a space qualifiable mixed signal payload data processor ASIC, and have introduced the project consortium, the ASIC key components and the evolution from previous projects. The first milestone of the project has been fulfilled and the whole project will be completed within a two year timeframe, leading to the commercial availability of a new powerful DSP for space applications.

ACRONYMS

AMBA	Advanced Microcontroller Bus Architecture
COTS	Commercial Off-The-Shelf
DARE	Design Against Radiation Effects
DSP	Digital Signal Processor
EM	Engineering Model
ESA	European Space Agency
ECSS	European Committee for Space Standardization
GOPS	Giga Operations Per Second
GPP	General Purpose Processor
LEON	Not an acronym
MAC	Multiply ACcumulate
MPPB	Massively Parallel Processing Breadboard
NoC	Network On Chip
SPARC	Scalable Processor ARChitecture
SPI	Serial Peripheral Interface
SSDP	Scalable Sensor Data Processor
SpW	SpaceWire
SW	Software
VLIW	Very Large Instruction Word
V&V	Verification and Validation

REFERENCES

1. JUICE Assessment Study Report, Jan 2012, http://sci.esa.int/science-e/www/object/index.cfm?fobjectid=49837
2. JS-14-09 *JUICE Environmental Specification.* Issue 44, Revision 99, 15 January 2012.
3. Massively Parallel Processor Breadboarding Study, ESA Contract 21986, Final presentation, available at http://www.spacewire.esa.int/edp-page/events/ESA_DSP_Day_-_August_2012.htm
4. Multicore SoC for On-board Payload Signal Processing, Adaptive Hardware and Systems Conference, San Diego, USA, 2011.
5. ESTEC Contract 15852/01/NL/FM, Executive Summary, Low Power, Radiation Tolerant Microelectronics Design Techniques. http://microelectronics.esa.int/finalreport/DareExecutiveSummary_V3.pdf
6. TEC-EDP/2008.18/RT - Next Generation Space Digital Signal Processor Software Benchmark, Issue 1.0, 01 12 2008
7. ESA IP core service, ESA Microelectronics website http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html