RELATION BETWEEN DEGRADATION OF ELECTRICAL PARAMETERS OF MOS TRANSISTORS BY HOT CARRIER INJECTION AND THEIR DRIFT DUE TO RADIATION FOR A NEW RADHARDENED ACMOS FAMILY.

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Abstract - **Space environment induces degradations, which affect electrical performances of MOS transistors in satellites. It is very interesting to prevent such degradations, to be more competitive and to mainly satisfy customers in the best conditions. But the tests by ionizing radiations are long and expensive. That's why we would like to predict the effects of radiation by using tests with hot-carrier injection. Indeed the degradations induced with hot-carrier and radiations effects are similar. Oxide is damaged by charge trapping and interface states generation. Electrical parameters such as threshold voltage, linear current and transconductance are affected. Our study consists to find a correlation between the degradations of MOS transistors induced with hot-carrier and their damages due to gamma radiation environment.**

Keywords – ACMOS Radhard, radiation hardness, hot carrier injection, Method1019.5.

I. INTRODUCTION

The identification of a relation between MOS transistors degradation due to hot carrier injection and their behavior under Co60 is an important economic challenge. This work has been performed on a newly designed ACMOS family for space applications of STMicroelectronics. Note that the hardening design approach performed on this family is fundamental: in other terms, the behavior of this technology under radiation is only driven by gate oxide performance. The two physical phenomena induced by hot carrier injection and by radiation exposure are similar: in the two cases the main effects are oxide-trapped charges in gate oxide and interface states generation. For hot carriers, the carrier injected in the channel becomes "hot" because of the high electric field applied on the drain; when their energy is higher than the one of Si/SiO2 barrier, some of them are injected into gate oxide. This injection impacts gate oxide quality by generating interface traps that degrade consequently electrical performances of the components (mobility, threshold voltage, drain current, transconductance…).

II TEST VEHICLE PRESENTATION

2.1 Radiation hardened technology

54ACMOS family is a sub-micron technology of **0.7µm** built on an **epitaxial substrate**. The behavior of such technology under Co60 irradiation is well known and the main parameter affected by such an environment is the quiescent supply current. The contribution of gate oxide appears at high total dose up to 100krad due to it thin thickness.

Radiation hardness of such a technology is difficult to address only with an appropriate process tuning that is the reason why STMicroelectronics has fight against radiation damages by developing a new design solution. One of the main advantages of this new design approach is the repeatability that STMicroelectronics is able to guaranty from one production lot to another.

With this design approach, STMicroelectronics is able to propose a 54ACMOS family at 300Krad of total dose according to ESA/SCC specification 22900 and also MIL-STD-883E T.M. 1019.5 method. The test vehicle used for this test is a standard gate coming from a RADHARD diffusion lot issued from the new design. Radiation response of this radhard technology is resumed to gate oxide behavior. Different radhard trials have been carried out for evaluation of dose rate effects, burn-in effects and polarization influences.

As far as bias conditions are concerned, two kinds of polarization to test total dose immunity till 300 krad have been used. For the rest of the trials, only the worst case of biased has been kept.

2.2 Test vehicle description

During the design kit validation of STMicroelectronics, a test chip containing radhard elementary cells has been

developed in order to carry out radiation tests and also heavy ion injection tests. The test vehicle chosen is a NMOS radhard transistor present on each wafer lot production of STMicroelectronics.

III. DEGRADATION MODES

3.1 Hot carrier injection mechanisms

3.1.1 Introduction

The new advanced submicronic technologies tend to minimize size of elementary transistors more and more. One of the associated troubles is the huge increase of the electrical field in the transistors that generates hot carrier generation and could affect reliability of the component.

3.1.2 Physical phenomenon

When dimensions of the transistors tend to decrease with a constant value of power supply, the lateral field associated increases. If this electrical field becomes critical, parasitical phenomenon can be generated and affect electrical parameters of elementary cells such as threshold voltage, transconductance, linear drain current…
When the elementary transistor is saturated, the maximum electric field is given by:

$$E_m = (V_{DS} - V_{Dsat})/m$$

where $m = 0.22 t_{ox}^{1/3} / x_j^{1/2}$
With t_{ox} : gate oxide thickness
$x_{j\ :\ Drain/substrate}$ junction depth
$V_{Dsat} \approx V_G - V_T$

When the electric field reaches a critical value dependent of biasing conditions and physical layout of the elementary cell, some electrons of the substrate become "hot ": they acquire an important kinetic energy and are no more in thermal equilibrium with the lattice. These electrons are called « hot carriers ». The sensitivity to this phenomenon for NMOS transistors is due to a higher mobility of electrons compared to holes.
The application of an important electric field to a NMOS transistor induces two major effects: the first one is the apparition of a substrate current and the second one is the injection of carriers into gate oxide.

Substrate current

When the value of the electric field permits the generation of « hot carriers », the carriers acquire a sufficient kinetic energy (greater than 1.5eV) to generate electron/hole pairs by ionization during the impact of the atoms of the lattice. These created pairs generate a substrate current Isub. When Vds is greater than Vgs more specially when drain voltage is at its maximum, the electric field at drain level increases the ionization by impact. The most energetic carriers created can be injected at the interface Si/SiO2 and in gate oxide helped by appropriate biasing conditions also on the gate (Figure 1).

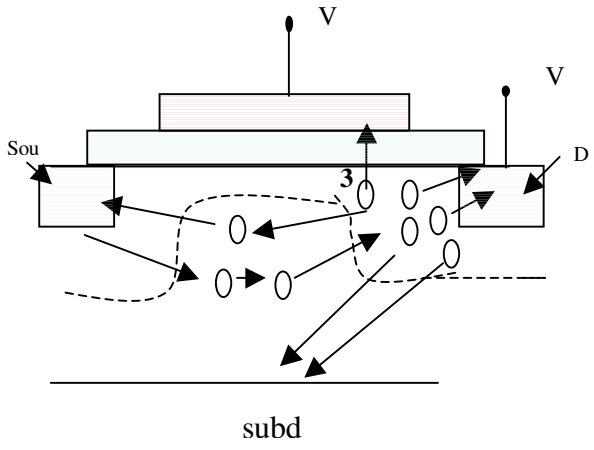

Figure 1: Gate oxide injection by substrate current

This injection of « hot carrier » methodology has been discovered by NING on a NMOS transistor: the resulting model name is « lucky electron ».

Hot carrier injection in gate oxide

When kinetic energy of « hot carriers » reaches energy higher than the one of Si/SiO2 (3.2 eV) barrier, these carriers are injected in the gate oxide. The resulting effect is the generation of a gate current without any effect on reliability of the component. Little part of "hot carriers" tends to be trapped in oxide and a resulting fix charge appears in the oxide or near the interface S_i/S_iO_2.
The injection in the channel depends of gate bias conditions. For a MOS transistor working in a saturated mode a high lateral electric field is present near the surface of the channel. Figure 2 illustrates this phenomenon. Note that the transfer of the carriers is limited .

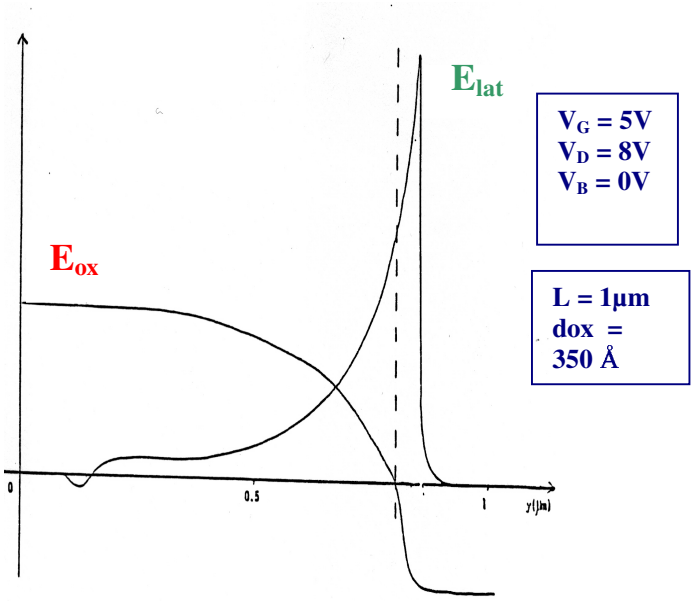

Figure 2 : Comparison between lateral electric field (Elat) at the surface and electric field through the oxide (E_{ox}).

On figure 3 the lateral electric field is represented with the transversal electric field (through the oxide) for a NMOS transistor biased with $V_D > V_G$.

Current flow in the transistor
Hot carrier injection in oxide
Electric field in the oxide

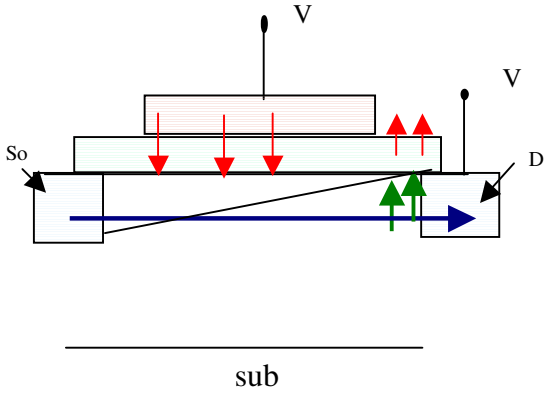

Figure 3 : Schematic representation of hot carrier injection coming from the channel current.

In a NMOS transistor, the holes participate to the substrate current Isub, the injected electrons to the gate current Ig. "Hot carrier" injection alterates oxide quality by the generation of interface states and trapped charges. These defects are localized near the drain region and the main consequence is a degradation of mobility, threshold voltage, linear drain current and transconductance.

3.2 Degradation by radiation

The dose is defined as the deposit energy in a material per unit of mass. This deposit energy is able to modify the electrical characteristics of a component. If no specific design and/or process modifications are performed, even a small dose is able to modify the electrical behavior of an IC. In space environment, the average deposited dose is very poor around 1 rad/h. If we take into account this poor dose rate, the effects in the silicon can be ignored. On the other side, the effects in oxide are important and able to trap charges for a long time. The degradations due to total dose are linked with charge accumulations in oxides and interface oxide/semiconductor. The main troubles, in a MOS transistor are the increase of leakage current, the drift of threshold voltage and also modification of transconductance. The quantity of trapped charges in volume is proportional to the square of the gate oxide thickness. So the thinner is gate oxide, the minimum is the drift of the threshold voltage. Besides, if the thickness appears as a major contribution, oxide quality is also important for a good behavior under radiation.

The two degradation methods, "hot carrier injection and total dose degradation induce similar behaviors in term of electrical performances, so a comparison on affected parameters can be performed.

IV. EXPERIMENTS

4.1 Irradiation campaign

The irradiation phase took place in ORIS Labra using a CO60 source. The components used during irradiation have been biased using the worst case known. The characterization done after radiation has consisted in analyzing the percentage of degradation of the linear drain current that is known to be affected by radiation campaign. The curve here below on figure 4 is representative of the degradation of this electrical parameter after 200Krad of total dose. The parts have been irradiated according to method1019.5. This experiment is not detailed because well known of radiation community.

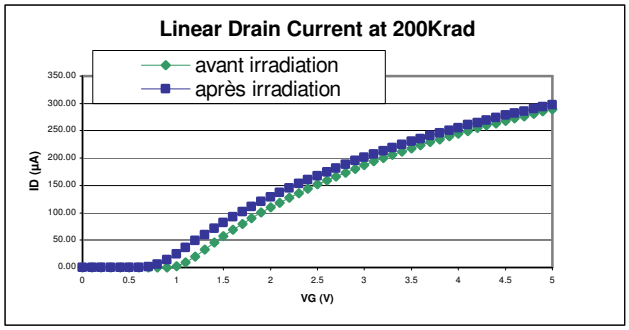

Figure 4: Degradation of linear drain current

4.2 Set-up of degradation by "Hot carrier injection".

The study of degradation by hot carrier injection leads to estimate the reliability of MOS transistors. The evolution of this parameter is very important during dice manufacturing to detect any drift of gate oxide quality. The model used for degradation of MOS transistors is the TAKEDA model defined as follow:

$$\frac{\Delta Idl}{Idl} = \exp\left(-\frac{a}{V_{Dstress}}\right) t^n$$

t : time
$V_{Dstress}$: Threshold voltage applied on the drain
a,n : Experimental parameters for each technology
Idl: Linear drain current.

The $\Delta Idl / Idl = f(\log t)$ curve of figure 5 represents the stress time needed to reach 10% of degradation for the electrical parameter chosen as the most critical one under radiation. This degradation of 10% corresponds to a lifetime of ten years for the component (value fixed by STMicroelectronics).

In our case, when the ACMOS technology (0.7µm) is submitted to radiation one of the most electrical parameter affected is the linear drain current which is linked to the threshold voltage drift.

Degradation results for different stress voltages

Measurements are performed at different drain stress values from 6.5V to 9V with V_D/V_G around 2.8. The exposure time is calculated in order to obtain 5 measurements values per decade. The cumulated stress time varies from 100000s for stress voltages of 9V, 8.5V, 8V, 7.5V to 200000s for a voltage of 7V and 6.5V.

The results are presented on the following table:

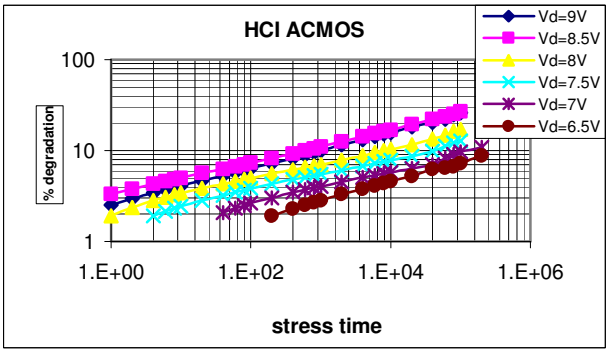

Figure5: Degradation of ACMOS technology for different stress values

For each stress voltage applied, we remark that the slope of the different curves are identical and present a shift toward the minimum value of the time when V_D stress voltages increases. The slope of the curve characterizes the kinetic of failure of the elementary cell. The degradation observed on the curves is homogeneous which indicates the good level of reliability and maturity of the technology in terms of design and process.

For each stress value, we have plotted the regression curve to deduce the extrapolated time corresponding to 10% of degradation of the linear drain current (Table 1). These results are very important because they will be used to establish the correlation with the irradiation campaign.

The regression curves are driven by the following equation y=a.x+b.

	Idl		
	b	a	R^2
stress 0 : V_{DS}= 9V	0.410136	0.197596	0.999746
stress 1 : V_{DS}=8.5V	0.515698	0.178357	0.999499
stress 2 : V_{DS}= 8V	0.338195	0.173143	0.997304
stress 3 : V_{DS}= 7.5V	0.214957	0.173929	0.997776
stress 4 : V_{DS}= 7V	0.048372	0.18207	0.996524
stress 5 : V_{DS}= 6.5V	-0.18625	0.210785	0.998662

Table 1: Regression coefficients for different Vd stress

Time for 10% of degradation
959
515
6576
32248
166282
418267

Remark: the extrapolated stress time at 10% is higher for a stress voltage of 9V than for a stress voltage of 8.5V. This difference is due to the current clamp of the tester.

Maximum operating threshold voltage.

The study of the degradation by hot carrier injection leads to estimate the maximum operational voltage for a lifetime of 10 years ($3.2*10^8$ sec). For the qualification of the technology to this method of degradation, the operational voltage found by experiment must be higher than the real operating voltage written in the specification. For ACMOS technology, Vop is 5V.

The following curve presents a summary of the extrapolated time for 10% of degradation $t_{10\%}= f(1/V_{Dstress})$.

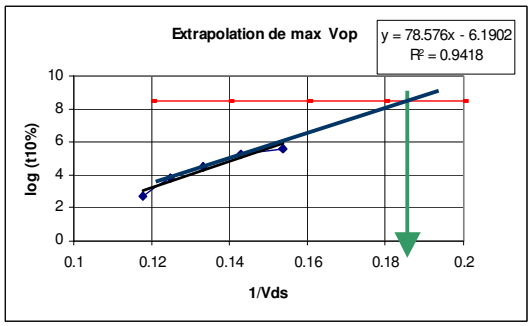

Figure 6 : Extrapolation of maximum operating voltage

The extrapolated equation (black line) is the following one:

$$\log(t_{10\%})=78.576*(1/V_{Dstress})-6.1902$$

So, we can easily deduce the maximum operating voltage.

$$\frac{1}{\max Vop} = \frac{(\log(3.2*10^8)+6.1902)}{78.576} = 0.187$$

The maximum operating voltage is 5.4V. This result is coherent because the maximum Vop found is higher than the real operating voltage of the specification. This result is a key factor that qualifies this technology to the degradation methodology by hot carrier injection. We can now go on with the job by determining a "short degradation methodology".

Definition of a short method

Degradation measurements by hot carrier injection require a long time to finalize that is the reason why to be sure of the reliability of the components and to detect some unexpected process drifts, many accelerated tests must be investigated and implemented. These "short-stress tests" take place in the program of cost reduction and also permit to have a rapid control of the reliability of the components. That is the reason why the second part of the job will deal with the determination of a "short-stress time method". The job is focused on the correlation of the percentage of degradation of the first short stress time (2s) with the time extrapolated corresponding to 10% of degradation of the most critical parameter previously chosen.
When the correlation will be established this "short-stress time" will permit to evaluate the total dose level of our technology with a very quick measurement.

Referring to TAKEDA model for p% degradation we obtain the following formula:

$$p\% = 10\% * \left(\frac{t_{p\%}}{t_{10\%}}\right)^n$$

This equation is completely independent from stress voltage so, for each stress level and for each technology, it exists a relationship between the degradation at the end of the first stress time and the time necessary to reach 10% of degradation of the most critical parameter. In the case of the ACMOS technology we found a law that correlate the measurements "long time"&" short time". The first stress time $t_{p\%}$ considerate is of 2 seconds.

To obtain the famous law, we tested all the dice on two wafers. Each die has been stressed during 600s with stress voltage of 8.5V. The quantity of stressed dice has reached 400 unities. After three days of test, all the results have been collected in order to deduce the extrapolated time corresponding to 10% of degradation. All the results are concentrated in the following table:

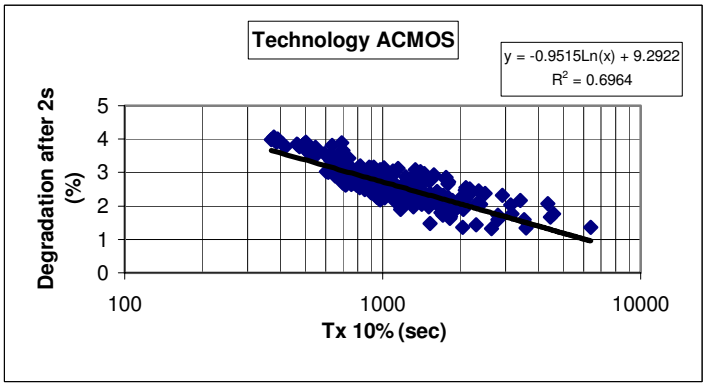

Figure 7: Correlation « short-time » « long-time » for ACMOS technology

We notice on this graph two distinguish populations. One reveals that an error has occurred that is to say that the tester had reached the clamp for some tested components so this population has not to be taken into account.

If we consider now the black distribution we notice that a correlation exists between the extrapolated time corresponding to 10% of degradation of the most critical parameter with the percentage of degradation at the end of the first stress after 2 seconds.

This correlation between « long stress time » and « short stress time » gives an estimation of MOS transistors reliability just by recording the behavior of an electrical parameter after few seconds of stress by hot carrier injection.

The final part of the job is to establish according all the experimental results a relation between total dose, stress conditions and polarization and the extrapolated time corresponding to 10% of degradation.

V. DISCUSSION.

We have demonstrated for ACMOS technology that a correlation law exists between the extrapolated time corresponding to 10% of degradation for the most sensitive parameter and the percentage of degradation at the end of the first stress « short-time » of 2s. This law that has been obtained by testing a huge quantity of components covering all the ACMOS technology that is to say all types of the family. An equivalent law for any kind of technology (MOS technology rad-hardened by design) could be determined if necessary, each law will be representative of a dedicated technology.

Let's summarize the way we can determine the total dose level of the ACMOS technology by stressing few components during 2s. By stressing an elementary cell representative of the ACMOS technology during a "short-time" (2s) we can determine the extrapolated time (long-time) necessary to reach 10% of degradation of the most critical parameter. In the typical case of ACMOS technology, we reach 3,33% of degradation after 2s of degradation that corresponds to 526s of stress to reach 10% of degradation.

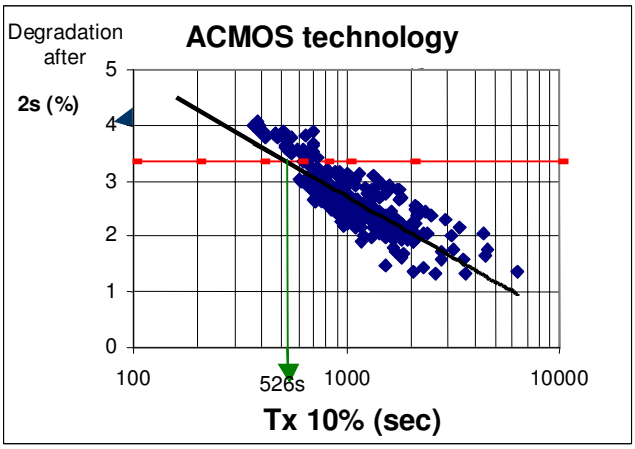

Figure 8: Correlation « short-time » « long-time »

When « long stress-time » is determined (526s in our case) and if we use the correlation curve obtained on figure 9, we can determine the total dose level reachable by the ACMOS technology.

The radiation results presented here below are post-radiation data: no annealing has been performed on the irradiated samples.

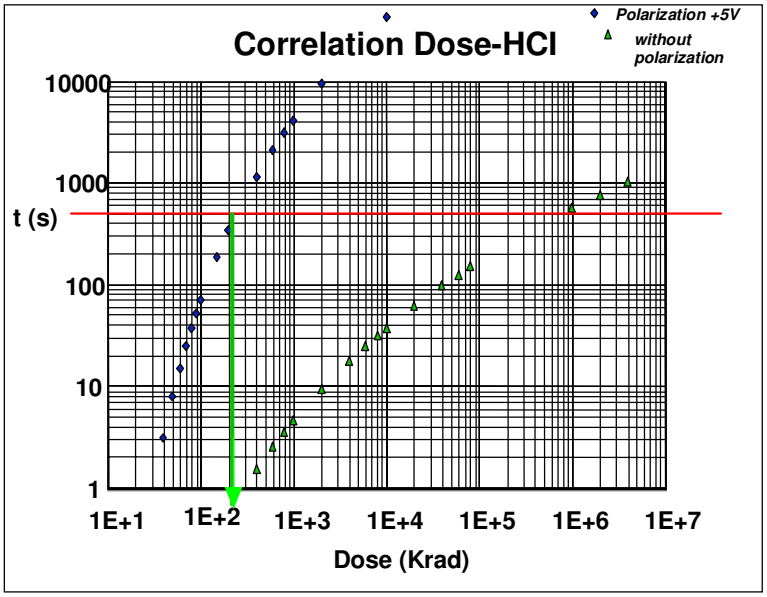

Figure9: Correlation Dose /Hot carrier (ACMOS)

The result is obtained for 10% of degradation of the most sensitive parameter (the linear drain current) that is also the maximum of degradation tolerated by STMicroelectronics for a lifetime of 10 years. These results could be adapted to another percentage of degradation if required by a customer or a product specification.

For ACMOS technology, the correlation law is expressed as follow:

$$LOG(D)=(1/a)*[t^{a}*exp(-a/V_{dstress})-b]$$

a and b are technology dependant and D is the total dose level.

VI. CONCLUSION

These evaluation results confirm that a relation exists on the degradation modes to have a real behavior of gate oxide response under radiation. In order to apply this new test methodology on production lots, a complete characterization has to be performed on each technology in order to determine the dedicated relation of the technology under study. This correlation is only available for gate oxide response and doesn't give information on leakage that could appear under radiation. The family under study has to be a radhard family in order to work on a design without any leakage current.

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