# Reliability Evaluation of Components for the Chip on Board (CoB) Technology in Space Application

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## Abstract

The paper gives an overview of the reliability evaluation of dice used in Chip on Board Technology (CoB) and gives an assessment regarding the experience gained for application of CoB in space designs.

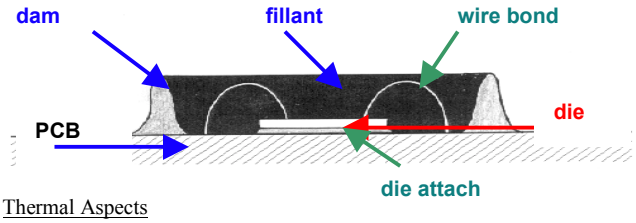
## 1. Introduction

Striving for smaller, lighter, better and cheaper products leads to the growing trend of miniaturisation of electronic hardware. The use of unpacked dies in a CoB type of assembly technology provides a reduction of at least 20% in assembly space. Due to this advantage CoB has already entered the automotive industry in high quantities. Preferred application there is e.g. for car radios. But even automotive applications with stringent reliability requirements are today realised in CoB technology.
Space grade EEE parts should be capable from a construction and reliability point of view to satisfy hi-rel application requirements. To evaluate the performance of CoB technology in a long term space mission, a reliability evaluation of CoB, which contained typical hi-rel screening flows, has been performed. This evaluation contained test sequences, which should show the compatibility between CoB and die. The evaluation was done on separate boards containing a single chip in CoB technology. This paper describes the reliability investigations for dice in CoB technology for space application. The investigations covered endurance, electrical, thermal and radiation aspects.

## 2. Description of CoB Technology

For the evaluated CoB technology, dice, with the circuit side up, are directly attached to an epoxy FR4 printed circuit board (PCB) with an adhesive. Followed by wire bonding (aluminium wedge) from die to pads on the PCB. This assembly is then covered with an epoxy sealant, the so-called glob-top. In order to fabricate the glob-top a ring of high viscosity epoxy (dam) is laid around the area, which is to be covered. Second it is filled with a low viscose second component (dam and fill, Fig.1). The covered assembly is then cured in three steps. No soldering steps are involved in the complete process. With glop-top coverage a hermetic package is not obtained. A sketch of the CoB type of construction can be seen in Figure 1 .

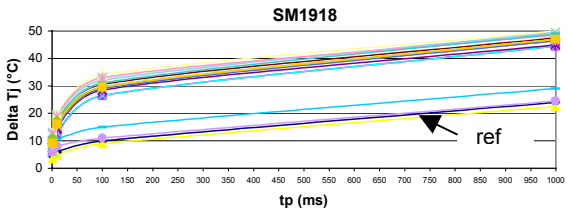
Figure 1 Schematic of CoB Technology (dam and fill)




Thermal Aspects

Due to the small size of most of the dice, the adhesive attach is not only a mechanical fixation, but also has to function as thermal heat path for the dissipated power, as only little power is dissipated through the glob top. Compared to packaged devices with eutectic or metallurgical die attach in metal or ceramic housings, the COB assembly on an epoxy FR4 PCB is a very sensitive construction regarding heat dissipation and applied power. This can be seen in the subsequent Figure 2, where the junction temperature versus heating pulse times is drawn. The tested part is a standard diode from Microsemi (SM1918). The diagram shows a comparison between an SMD type of diode (designated as “Ref” in the subsequent Figure) and the same chip assembled in a COB type of technology.

Figure 2 Junction Temperature versus heat pulse length




The tailored Evaluation program reflected this important difference. Therefore the applied Burn-in testing was performed apart from DC conditions also with current pulses as described below.

Inspection and Rework

PCBs with applied glob top are rejects if they fail the first electrical test. No rework is possible after application of the glob-top. In complex designs the question of the yield of the finally assembled PCB becomes an issue. Therefore the Inspection steps including electrical measurements prior the application of the glob–top must be carefully tailored with respect to the complexity to the design.

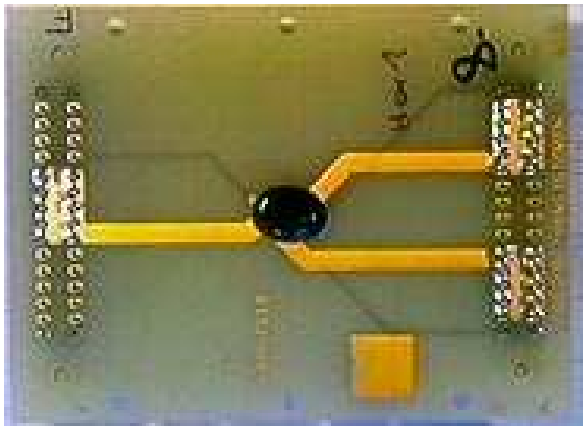
## 3. Used Dice and Materials

Dice

For the evaluation different part types were selected in order to have representative technologies, which are typically being used in DC/DC converter designs, under investigation. This has led to the selection of Bipolar and Schottky diodes as well as power FETs. Bipolar transistors and operational amplifiers are other examples of the evaluated part types. The intention was to be able to extend the results to a wide range of possible dice by similarity.

The used quality level was of a military grade. The dice were procured according to level H of MIL-PRF-38534. No Known Good Die approach was used.

Figure 3 Typical appearance of a test sample



The used types and manufacturers can be seen in the table 1 below.

Table 1 Used part types for evaluation testing

| Type | Family | Manufacturer |
|---|---|---|
| FSC110S | Hexfet | Intersil |
| 2N2222AHR | Transistor | STM |
| 2N2369A | Transistor | STM |
| MD1918 | Diode | MSC |
| MD4962-13 | Diode | MSC |
| MD4469-12 | Diode | MSC |
| 1N5819 | Diode | CDI |
| OP43-036C | IC | ADI |

## 4. Evaluation Investigations

The evaluation program was divided into three subgroups. This can be seen on Chart 1 subsequently. **Subgroup 1,** the endurance subgroup, was tailored to evaluate the mechanical configuration of the assembly. Thereby the question of the impact of the different thermal expansion coefficients of the silicon chip with respect to the glob-top and the FR4 PCB was the most prominent concern.

The intention of **subgroup 2,** the electrical subgroup, was to apply to the assembly a sequence of tests, that is similar to the screening of discrete parts during a space level screening. The CoB type of assembly has compared to a discrete hermetic package two important differences. The first difference is that the PCB must not be heated to over 100°C. This means the thermal stress conditions applied during testing must take this factor into account. The second difference is that the thermal resistance between the junction and a heat sink is higher due to the isolated nature of the CoB package. Therefore the stresses in **subgroup 2** contained, apart from normal dc type of burn-in and life tests, also pulse tests. By selecting a suitable pulse length a situation can be generated where the junction of the semiconductor is heated up, while the PCB and the Glop-top stay at the test temperature level. This results in a different stress scenario compared to normal dc stress conditions.

**Subgroup 3,** the radiation subgroup, was designed to review the impact of the glob-top on the sensitivity of the semiconductor to radiation. The trapping of charges in the coating material was the biggest concern, which has led to this sequence of testing.

## 4. Results

In the following, summaries of the gained results are provided for the different types. The results obtained on subgroup 1 and 2 are reported in respect to their part category. Each block starts with as short description of the used test vehicle. Due to the specific nature the Radiation aspects are reported in a separate block.

MOSFETS

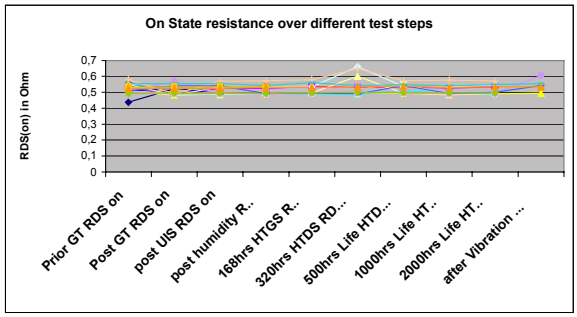
Dice with three different sizes have been investigated in the endurance subgroup. The largest die in this evaluation was a die size 5 with an area of around 5 x 5mm. After the endurance tests no catastrophic or parameter failure was observed. However a slight degradation of the RDS(on) could be detected on the size 5 dice.

In the electrical subgroup only size 1 dice were investigated. Here again no failures occurred. However as in the endurance subgroup, the RDS(on) showed slightly higher values after drain stress life test and during the pulse tests also a slight increase of RDS(on) could be noticed.

Thermal resistance measurements showed about 2x higher values for the CoB than for units in TO254 package.

In Figure 4 a typical RDS(on) over different test steps can be seen. The first measurement are made prior an application of the glop-top. This test was repeated after the application of the glop-top and followed by further electrical measurements at various points during the reliability sequence. The measured electrical parameters were very stable. An example can be seen in Figure 4

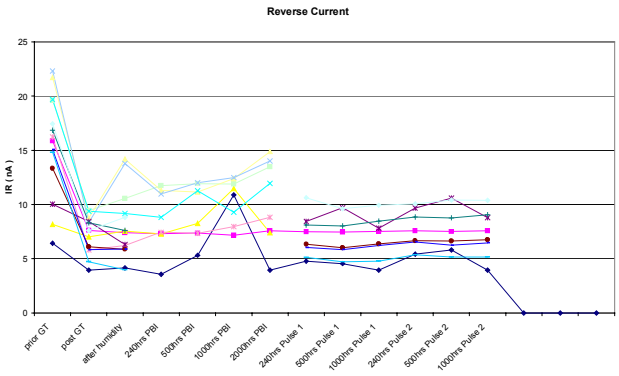
Figure 4 RDS(on) over different test steps on a powerfet hexsize 1



DIODES

Zener, Schottky and Rectifier Diodes have been investigated. The endurance subgroup showed no relevant electrical parameter changes. In the electrical subgroup decrease of reverse current of the Zener and the Rectifier diodes was observed after application of the glob top.

Figure 5 Zener diode 1N4469 reverse current over time

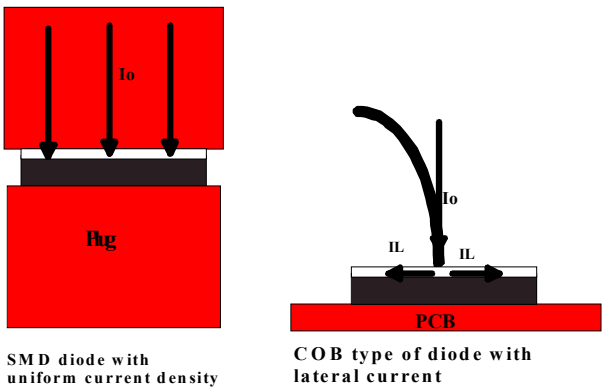



The values, however, remained stable during the evaluation. High temperature measurement of reverse leakage current of the rectifier diode showed a tendency to decrease over the evaluation. With the exception of Schottky diodes no remarkable difference of the individual electrical parameters of packaged units and CoB mounted samples were evident for all part types. For the Schottky diodes, however, differences in parameters were observed. A slight increase of the reverse bias leakage current was measured for this diode type after application of the glob top. During evaluation the increase continued, but overall the parameter did not exceed the specified maximum limit.

Figure 6 Reverse Current for the Schottky diode 1N5819


High temperature measurements showed a decrease of the reverse leakage current over the test period in subgroup 2. The special construction of the Schottky diodes with a semiconductor-metal barrier makes this type very sensitive to the used bonding configuration. Lateral surface currents (IL of the subsequent drawing ) have to be minimised by placing the bond contacts in such a way to have an optimised current distribution through the metal contact.

Figure 7 Comparison of a SMD and COB mounted diode.




Measurements of the thermal resistance showed for all three categories (Zener, Schottky and Rectifier) a 2x to 5x higher Rth value than the respective packaged part

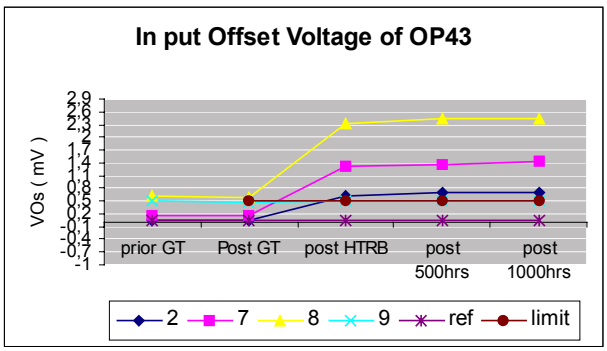
INTEGRATED CIRCUITS

During the endurance subgroup various ICs were investigated, whereas during the electrical subgroup only an operational amplifier was considered.

Failing of the input offset voltage occurred during endurance and electrical investigations on the operational amplifier. The internal design of the operational amplifier with a JFET on the input makes this part type very sensitive to the glop-top material. This is confirmed, as the input offset voltage increased significantly on some of the units after application of the glob top. Evaluating units with and without this deterioration, it was found that in case were the input offset voltage had started to increase after glob top application, the increase stayed stable at the same level over the complete subsequent test sequence.

In this operational amplifier design the balance of the two JFET input transistors is very sensitive by the applied glob-top. It is assumed that slight mechanical stress causes the shift in the input offset voltage. This is supported by the measurements over different test points, where no further degradation was observed. The behaviour of the Input Offset Voltage can be seen in Figure 8

Figure 8 Input Offset Voltage for the OP43



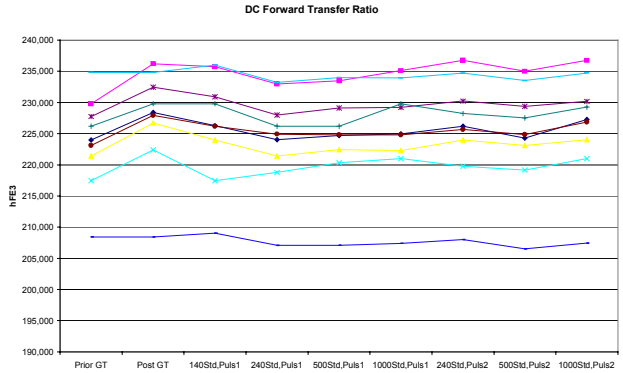
BIPOLAR TRANSISTORS

Two standard bipolar transistor types were selected for the evaluation (2N2222A and 2N2369). Parts submitted to the endurance subgroup showed no failures. In the electrical subgroup, a failure occurred after the first 240hrs of power burn-in (PBI). The part failed with a degraded VCE(sat). A failure analysis was performed and it could be demonstrated that the selected conditions for PBI produced an overstress to the adhesive attach of the assembly. The glass transition temperature of the adhesive is at 160°C. The failure analysis showed that this temperature was exceeded. A calculation demonstrated that it could have reached 199°C. The die attach quality was reduced and consequently the measured transistor parameters showed a degradation.

Because of this failure the evaluation was re-started with optimised conditions and a temperature sensor was added underneath the chip. Care was taken, that the die attach was not heated above 150°C. The second evaluation passed without any failures. Between the packaged units and the CoB mounted units slight parameter differences of the breakdown voltages and saturation voltages were measured.

In Figure 9 the hfe distribution over different test steps can be seen.

Figure 9 2N2222A hfe over different test steps (With optimised test conditions)




The thermal resistance measurement showed high variation of results depending on the test conditions. The evaluated maximum Rth was determined to be 126K/W.

RADIATION SENSITIVITY

A bipolar transistor and an IC ( the operational amplifier ) were tested to evaluate if the CoB technology has a influence to the radiation behaviour. This was not the case. The transistors could be irradiated up to 100Krad(Si) total dose without significant changes. For the hfe the typical degradation for bipolar transistors could be seen (Figure 10 and 11).

Figure 10 Monitoring of the parameter hfe for 2N2222A(IC=1mA, VCE=10 V)

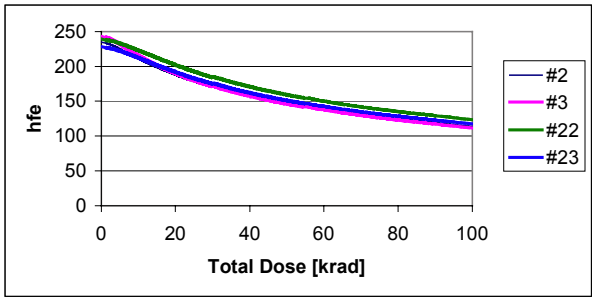
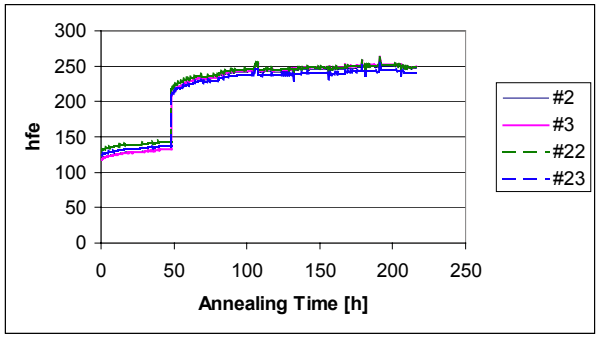



Figure 11 Monitoring during annealing




After Annealing the degradation recovered completely to the original values. For some parameters the recovery was to 80%of the initial values

The operational amplifier was irradiated up to 40Krad(Si) total dose without significant degradation.

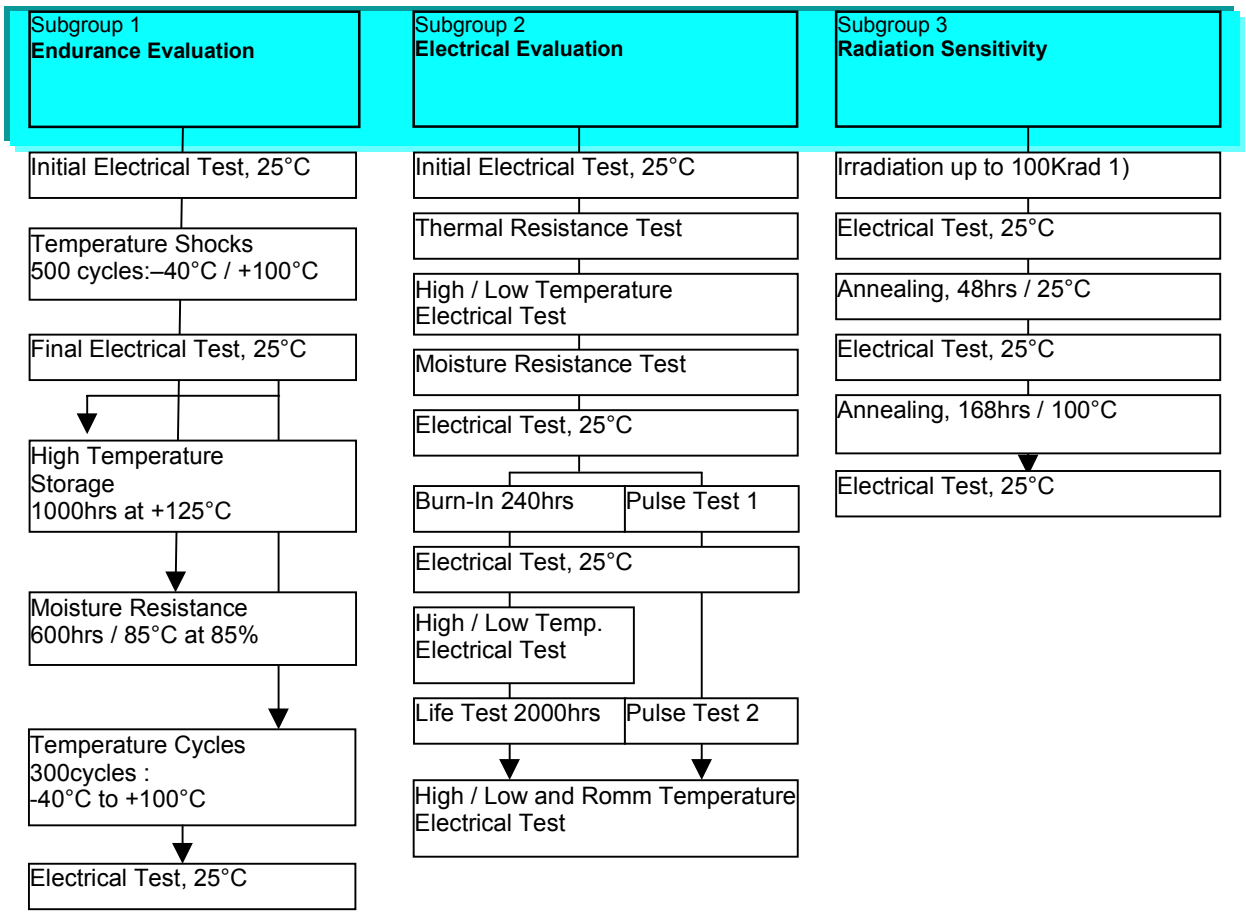
## 5. Conclusion

The main focus at the reliability evaluation was to find out the performance of dice mounted in CoB technology under endurance and electrical conditions, that simulate the qualification stress level for a space mission. The results demonstrated that CoB is a reliable assembly technology. After selecting appropriate stress conditions during the testing, no catastrophic failure throughout the entire evaluation could be generated. The observed degradations were component type dependent. It is therefore recommended to verify the compatibility of the CoB technology on each new part type not covered by existing data.

The evaluation however demonstrated on the other hand that the CoB technology is very sensitive regarding thermal aspects, when the technology has to work under high power conditions. Local temperature effects must be considered by the design. New derating requirements must be established for each family of devices.

Other aspects, which are also critical in hybrid type of technologies must be considered in the CoB technology as well. For example bonding distribution over active areas and current-driving pads has to be carefully selected for the design of CoB assemblies. Diodes with low forward voltage are an example of this case.

Chart 1 Typical Test Sequence for Reliability Evaluation




1) The 2N2222A was irradiated up to 100Krad, whereas the OP43 was irradiated up to 40 Krad.

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