An onboard FEC decoder for burst mode operation

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Abstract

Use of FEC in regenerative satellite communications systems with low signal to noise ratio requirements allows to meet a high quality of service (typically 10-10 BER). To carry multimedia information, burst transmission mode is usually preferred. Temic has developed a FEC decoder which allows to keep using a concatenated coding scheme (Viterbi plus Reed Solomon) while communicating in burst mode on satellite uplink.

Introduction

More and more satellite digital telecommunication payloads are expected to operate in a regenerative mode so as to accommodate the stringent requirements of ground portable sets power limitations and of Ka band propagation requirements, imposing to reach good Bit Error Rate at always lower signal to noise ratio.

Temic, with the European Space Agency funding and the support of Alcatel Space Industries for the system requirements, VHDL and silicon validation phases, has developed a Viterbi and Reed Solomon decoder to answer this demand. The performances of those functions will be presented in this paper regarding the existing implementation on Temic MG1RT sea of gates series, together with its expected improvements, when implemented on a 0.5 µm RT standard cell library.

Moreover the decoder design has been adapted to a burst mode operation, to allow the use of the developed chip in satellites as those operating with OBP TDMA access schemes.

Eventually, this program has been funded by ESTEC n° 12020/96/NL/NB in the frame of 2 contracts, the first one for the modelization, the design and the manufacturing of the chip with Temic MHS as prime, and the second one for the models validation with test vectors, and the chip in system validation with Alcatel Space as prime.

Standards compatibility

Designed for space applications, it conforms to:

- the **CD 13818-1 MPEG-II** transport layer protocol standard specified by the ISO and IEC organizations,
- **ETS 300421FEC** requirements of Digital Video Broadcasting (DVB) and Digital Video Broadcasting Satellite(DVB-S) specifications.

As such, it is suitable for applications such as DVB, regenerative multi media transmission satellites and military applications.

Supporting technology and product

The chip was designed on a Sea of Gates series manufactured an a radiation tolerant 0.6µm CMOS process, whose developments were respectively funded by CNES and ESTEC. It uses an MG1265E matrix allowing the routing of almost 190Kgates, packaged into a 132 pins multi layer quad flat pack.

The technology has been hardened to survive to latch up for heavy ions energy above 100 MeV/ mg.cm² and a total dose capability better than 100Krads when tested to SCC22900 conditions. The MG1RT Sea of Gates library encompasses a subset of cells which have been designed for being SEU free, and which will be used in this design where the SEU related errors occurrence would be higher than the Viterbi and Reed Solomon correction rate capability.

Eventually, effective December 10, 1999, Temic MHS has received the DSCC QML Q & V certification for the technology and the MG1RT series. An SMD number is now available as 5962-00B01.

Why a FEC decoder?

The market for satellites based communications evolves more and more towards a consumer type of approach, such as:

- Portable sets must be capable of being cheap, small size, small antenna, resulting in lower and lower signal to noise ratio, and very low emitted power,
- Satellite receivers can't operate at a reasonable cost with such very low power signals received from the portable sets,
- The limited available frequency spectrum combined with more and more new entrants is this market results into higher risk of frequency interference's, and therefore more noise,
- It is cheaper to deport more and more network management processing from the ground stations onto the payloads, which requires effective data integrity available on board of the satellites,
- The signals have to propagate in Ka and Ku bands, making them more sensitive to atmospheric conditions, resulting in additional noise.

Therefore the need for regenerating the data on board of satellites, and FEC, so far, have demonstrated their ability to achieve it with good track records, worldwide recognized standards, and therefore, documents and specifications for system designers allowing to design, manufacture and deploy systems which can understand each others.

Viterbi decoder major characteristics

The constraint length is directed by the DVB-S standard, and is equal to 7.

The input decoder is either hard decision, or 3 bit soft decision.

It is capable of regenerating data with a maximum 2^{E-4} BER with code ½, while operating in a 3.5 dB signal to noise ratio environment.

Reed Solomon decoder major characteristics

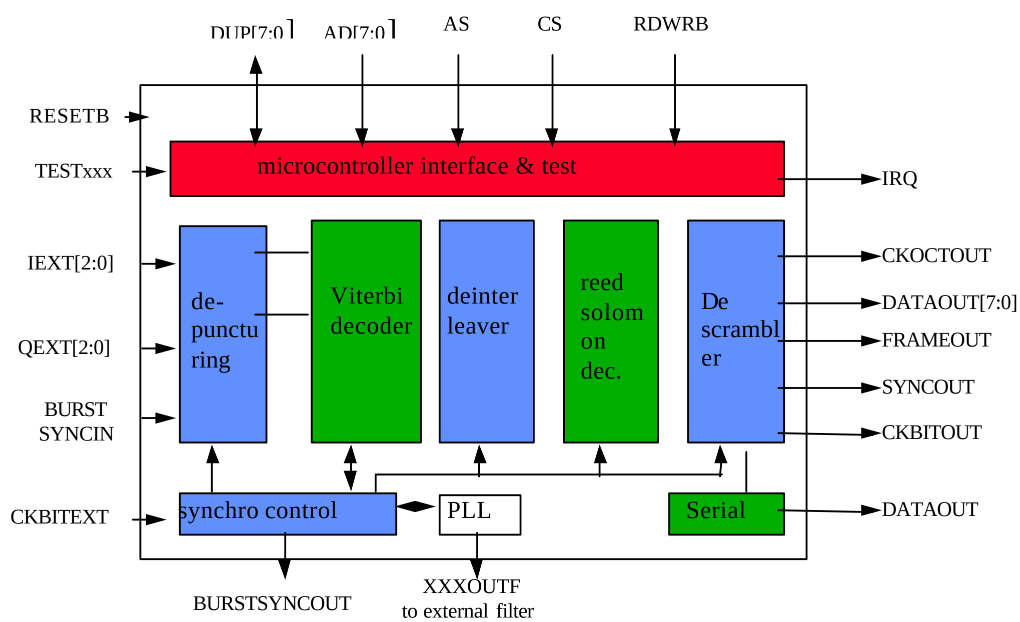
It supports programmable shortened code lengths K from 16 to 239 bytes, with a T=8 bytes correction capability, with 16 bytes check symbols.

Complete decoder chip major characteristics

So as to achieve a complete DVB-S decoding chain, we have added some of the mandatory features such as:

- Synchro controller, which is automatic when operating in the QPSK or BPSK modes,
- The selectable code rates are ½, 2/3, ¾, 5/6 & 7/8, and the decoder is capable of automatic acquisition.
- A I=12 de-interleaver,
- The de-scrambler for energy dispersal,
- And a micro-controller type of interface to allow chip programmation for the operation and the isolation needed for the characterization and test of each individual blocks.

The block diagram below describes the chip with its major functional blocks, and how they interface to each others.



Development methodology

The critical task was to start with an accurate and efficient description of the functionality of the chip, and this is why we used the C language which is more flexible for the optimization of major parameters such as **the treillis length,…** This is where were focused most of:

- our efforts so as to come to a C model validated with the Alcatel Space test file, when simulated,
- Alcatel Space added value was, as they are the ones who have the system knowledge and experience so as to properly generate test files with embedded noise so as to verify the correcting efficiency of our models.

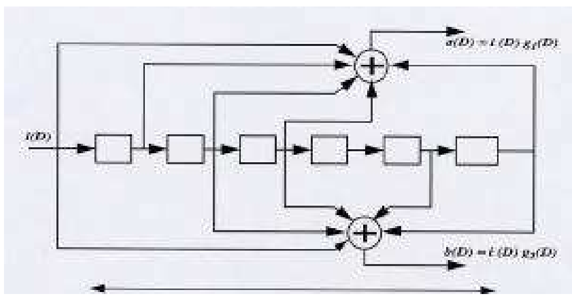
The next step was to convert the C models into VHDL models, with timing constraints, so as to start verifying the speed performance of each individual blocks, which were again validated with the Alcatel Space test files, converted also from C to VHDL files.

Then the synthesis was done, with also timing driven constraints, and the insertion of the SEU free cells allowing to provide the correction process with an high enough SEU related immunity, mostly in the treillis portion, but also everywhere some memory functions were implemented, and again, validation with Alcatel Space test files.

Eventually, it went through the regular ASIC back-end design flow such as placement, routing, clock tree synthesis, back annotation, timing analysis, design rules checks and layout versus schematic verification, and final verification against Alcatel Space simulation files.

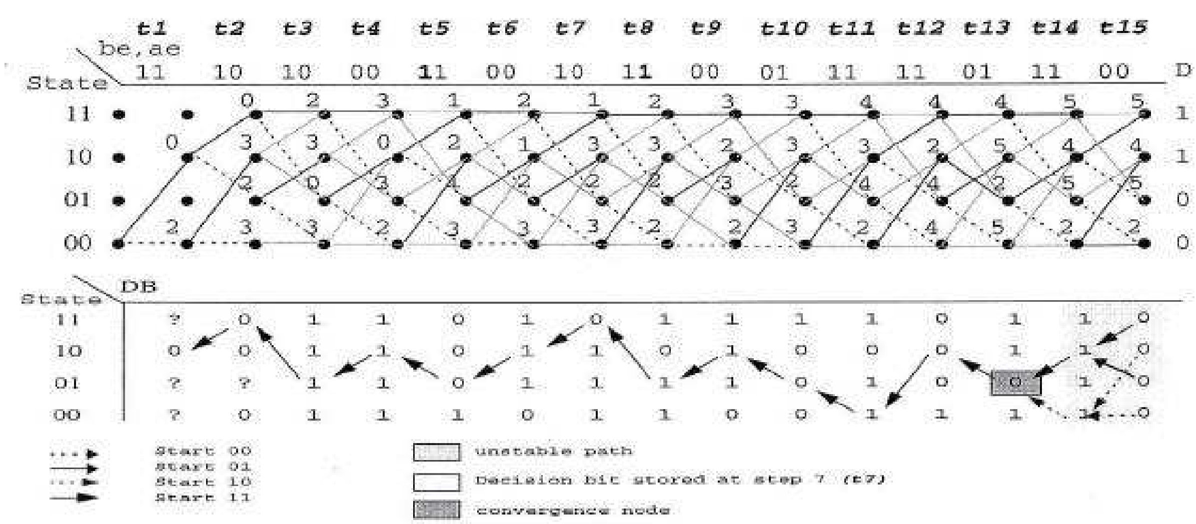
Reminder on Viterbi encoding

As shown on the following figure, it is based on a K=7 constraint length, which means that you need 6 levels of encoding/clocks or memory points before flushing out the data as a 2 bits symbol which will be, later on, punctured.



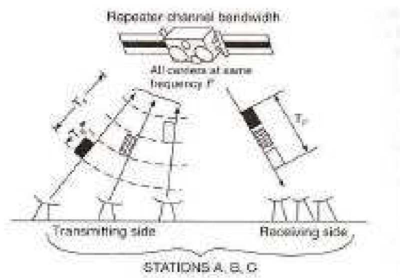
Reminder on Viterbi decoding

The following treillis describes, for an K=3 encoder, how the data propagates with the various options paths depending on former data, and which will result, at the end, in a deterministic value, when the transmission media is noiseless.



Burst mode: why?

This is mostly how multimedia communication satellites operate, being no longer point to point bent pipes, but active processor multi points to multi points communication channels, as the following figures put it in a simple manner, with mostly TDMA type of transmission channel access.



Burst: how?

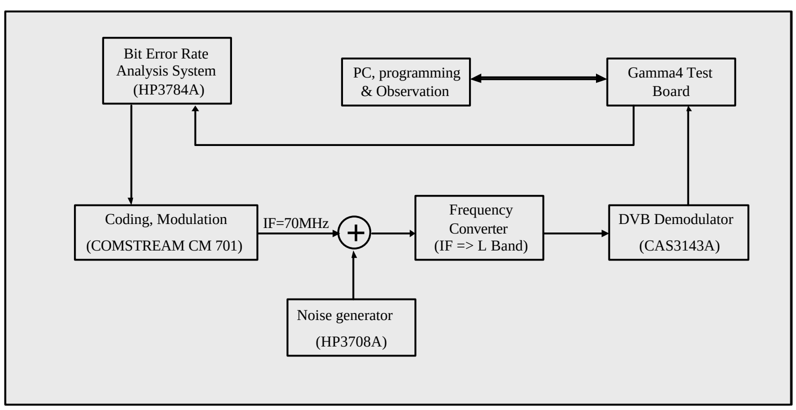
In fact, the recipe came from the following analysis:

- One need to flush the content of the encoder, therefore, feeding it with 6 data, for a K=7,
- One must guarantee the data continuity in the decoder treillis: this is achieved by enforcing the treillis in a steady state, “00” or “11”,
- One need to disregard the errors between 2 bursts; this is achieved by getting the data envelope.

Because we need to detect the burst operation, we elected the “00” steady state, directing the emitters to feed the encoders with 6 “0” on a row to flush the decoders.

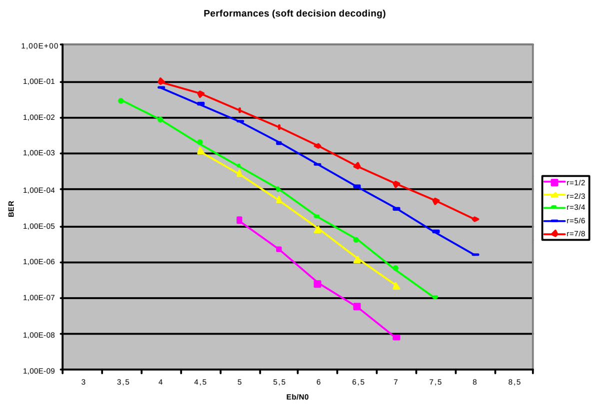
Alcatel Space chip validation methodology and results

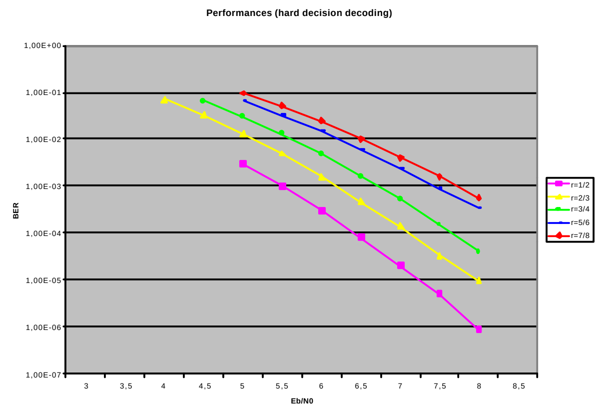
The following figure shows the block diagram of the hardware test bench.



Pseudo random data is generated through the Bit Error Rate Analysis system. This data represents the useful data. Data is then Viterbi (or DVB) coded and modulated, according to the functionality to be tested. Gaussian noise is added to the coded and modulated signal at an intermediary frequency of 70 MHz. The noise generator module allows Eb/N0 tuning. An IF translator is necessary to allow demodulation of the data via the Comatlas demodulator.

The following curves represent the useful Bit Error Rate (BER) measurements, done for different rates, imposed by the DVB recommendation. An important point to notify is the fact that all the curves take into account the demodulation loss.





Burst mode operation system implications

Burst mode operation can be achieved, providing phase ambiguities of the demodulation stage have been resolved. In the case of QPSK modulation, phase recovery can lead to demodulate symbols corrupted by a $\pi/2$, π or $3\pi/2$ rotation.

Phase ambiguities can be resolved using methods such as :

- Appropriated differential encoding of the data after FEC coding,
- Unique word transmission. Unique word is useful only for the demodulator. If no rate adaptation is done between demodulation and decoding, the validation flag at the input of the decoder must be kept low (inactive) while the input word gets into the decoder, consequently increasing the inter-burst length. Bandwidth is increased according to the overhead imposed by the unique word transmission.

Conclusions

Joint Alcatel Espace and Temic MHS work has resulted in a validated chip, the TSS902E, with a specification available for designers, and 2 programs (1 European, and 1 US) having already used it.

For the purpose of speed and power consumption improvement and minor bugs fix, we have re-synthesized the model on a 0.5 µm standard cell library whose main achievement should be to drastically increase the maximum input data rate to 52 Mbps at rate=1/2, while keeping the power dissipation at the same level.

Beyond the validation of each blocks constituting the available chip, an activity can be initiated for building a library of blocks to be used with any of our ASIC series, starting from the VHDL models for simulation, leaving our customers performing their synthesis. The Viterbi and Reed Solomon decoders candidates for our telecom oriented library of IPs.