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HISTORY AND ADVANCEMENTS OF LARGE AREA ARRAY SCIENTIFIC CCD IMAGERS

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ABSTRACT

This paper summarizes progress made in the past eighteen years in the development of the scientific charge-coupled device at JPL in collaboration with several CCD manufacturers and foundries. We examine advancements made since its conception, its current achievements, and report on new performance limitations for the sensor in the future. We discuss how these very useful devices work and examine new physical understandings behind their most remarkable characteristics. Some of these subjects include: array and pixel size, quantum efficiency, quantum yield, charge collection efficiency, charge transfer efficiency, read noise, dark current, full well capacity, anti-blooming, residual image, and tolerance to radiation damage. New test tools developed to measure these characteristics are also introduced.

1. INTRODUCTION

Charge-coupled devices (*CCDs*) were first introduced to the world in 1970 in a pair of papers by Boyle and Smith in the Bell System Technical Journal (1,2). CCDs were initially conceived as an electronic analogue of the magnetic bubble device. In order to function as memory, there must be a physical quantity which represents a bit of information, a means of recognizing the presence or absence of the bit (reading), and a means of creating and destroying the information (writing and erasing). In the CCD, a bit of information is represented by a packet of charges (electrons (e-) or holes (h+)). These charges are stored in the *depletion region* of a *metal insulator semiconductor (MIS) capacitor*, important CCD structures to be described below. Charges are moved about in the CCD circuit by placing the MIS capacitors very close to one another and manipulating the voltages on the gates of the capacitors so as to allow the charge

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to spill from one capacitor to the next: thus the name charge-coupled device (3). A charge detection amplifier detects the presence of the charge packet providing a useful voltage to the outside world. Charge packets can be created by injecting charge from a diode adjacent to a CCD gate. Like the magnetic bubble device, the CCD is a serial device where charge packets are read one at a time.

Although the original concept of the CCD was a memory device, it became immediately clear to a large number of workers in the semiconductor field that the CCD had potential uses that ranged far wider than simple memory applications. During the past two decades, the primary goal of CCD manufacturers has been to develop CCD sensors to replace tube type sensors (e.g., vidicon tube). The emphasis has been on realizing the CCD's advantages in size, weight, low-power consumption, ultra-low-noise, linearity, dynamic range, photometric accuracy, broad spectral response, geometric stability, reliability and durability, while attempting to match tube characteristics in format, frame rate, cosmetic quality, and cost. As a consequence, most home video cameras are now based on CCD sensors where only a few years ago tube imagers were mostly used. Photographic film is rapidly taking a back seat to the new sensor where solid state color CCD still cameras (e.g. 35 mm) are now commercially available (e.g., Cannon). Although relatively expensive, by the end of the century a low-cost color "instamatic" CCD type camera is expected.

Early Astronomy and CCDs

Astronomers, with their fundamental interest in the detection of photons from far away places, were perhaps the first to recognize the potential of the CCD for high quality scientific imaging. In comparison to photographic film and SEC vidicon tubes already in use, CCDs offered several benefits to the astronomer. In 1973, workers at the Jet Propulsion Laboratory initiated a program to develop high performance large area array CCDs, designed for space-borne navigation and imaging instruments. To promote interest about the CCD in the scientific community the JPL team built a *Traveling CCD Camera System*, the first of its kind, to be used at major astronomical observatories worldwide. At the time astronomers and engineers were not familiar with the new chip and were basically content with photographic films and vidicon tubes currently in use. JPL management recognized that scientists should become familiar with the capabilities and unique features of the CCD to help promote and support future NASA imaging projects for flight missions. Expeditions to various observatories with the new camera system paid off as the CCD performed beyond anyone's expectations. New scientific

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discoveries were usually made each time the camera system visited a new site.

Following these visits the demand for the CCD became intense among astronomers. Simply put, those who had access to a CCD chip had the advantage in generating new science. Astronomy would never be the same for the CCD was about to revolutionize astronomical instrumentation much as film did nearly 100 years ago. Within a few years the CCD became the sensor of choice at all major observatories (with the possible exceptions of Schmidt telescopes like the 48-inch Mt. Palomar telescope that utilize large photographic plates). Also CCDs utilized at small observatories could participate and produce new science that at one time could only be generated by larger telescopes. With a sensitivity of 100 times faster than film, it was clear that more data could be produced in a shorter period of time using a CCD. The new sensor immediately set new records in seeing the most distant and dimmest objects in the universe, objects that were invisible to film and tube type detectors before.

NASA Space-born CCD Imaging Missions

Following the introduction of the CCD to the scientific community several new NASA/JPL proposals were written and awarded in using the sensor in space-born imaging instruments. Many NASA missions currently in space are based on CCDs. For example, JPL's Wide Field/Planetary Camera (WF/PC I) on board the Hubble Space Telescope (HST) utilizes eight Texas Instruments 800 x 800, 15-micron *picture element (pixel)*, 3-phase CCDs (*TI 3PCCD*). Although the spherical aberration problem permanently built into the primarily 94-inch mirror of Hubble is significantly limiting scientific return, the cameras and CCDs are performing to expectation. For example, the camera has returned gorgeous color photos of the planets Jupiter, Saturn, and Pluto with 0.1 arc-sec resolution employing image processing techniques to remove the spherical aberration in the images caused by the mirror. New WF/PC II cameras currently under construction at JPL with built-in corrective optics will use new state-of-the-art CCDs fabricated by Loral Aeronutronic Inc. (formally Ford Aerospace in Newport Beach Ca.). The JPL Solid State Imaging (SSI) camera aboard the spacecraft Galileo in route to Jupiter uses a single Texas Instruments 800 x 800, 15-micron pixel, virtual-phase CCD (*TI VPCCD*). Galileo may too have a potentially dangerous flaw with its high-gain antenna which would significantly limit the number of CCD images sent back from Jupiter (the data rate of Galileo's working low-gain antenna is limited to only 10 bits/sec at Jupiter requiring several hours to send a single image). Currently Galileo's camera and CCD are functioning flawlessly generating excellent images of Venus, Earth, Moon and also a

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single image of asteroid Gaspra. Most of the asteroid pictures will be transmitted by Galileo's low-gain antenna when the spacecraft swings by earth a year from now before heading to Jupiter. The JPL Solar X-ray Telescope (SXT) camera aboard the Japanese Solar-A spacecraft utilizes a single 1024 x 1024, 18-micron pixel VPCCD to observe x-ray emission from the sun. This camera was launched in August of 1991 and is generating spectacular high resolution x-ray movies of the sun. A new CCD camera constructed last year at the Lyndon B. Johnson Space Center has recently been flown on the Space Shuttle (September, 1991, STS-48) for NASA's Electronic Still Camera Project (ESC). The solid state camera, a modified Nikon 35-mm body, utilizes a 1024 x 1024, 15-micron pixel Loral CCD. Numerous high resolution black and white images of the shuttle and astronauts were generated.

Other NASA missions that plan to use the CCD include MIT/Penn-State's Advanced CCD Imaging Spectrometer (ACIS) employed on the Advanced X-ray Astrophysics Facility (AXAF). The instrument will generate high resolution x-ray images of active galaxies, super novas, quasars, etc. and simultaneously measure the energy of incident x-rays. Several high performance 420 x 420 pixel CCDs fabricated by Lincoln Laboratory will be utilized in AXAF's focal plane. It is hoped that AXAF will be launched before the turn of the century. NASA's Mars Observer (MO) is a CCD imaging mission to planet Mars scheduled for launch next year (1992). The MO camera is being built at the California Institute of Technology using two linear Loral CCDs (1 x 2048 and 1 x 3456 pixels). NASA's two newest planetary missions are: Comet Rendezvous Asteroid Flyby (CRAF) and Cassini. CRAF will obtain close-up views of a comet (comet Kopff) and an Asteroid (to be determined) using three imaging cameras (referred to as the Imaging Science Subsystem (ISS)) that utilize 1024 x 1024, 12-micron pixel three-phase CCDs fabricated by Loral. The imaging cameras aboard Cassini are identical to CRAF except for the spectral filters used. Cassini also carries a small probe to image Saturn's large moon Titan. The probe camera will use a custom Loral 512 x 512 pixel CCD. Also an Italian instrument, the Visual and Infrared Mapping Spectrometer (VIMS) cameras on board CRAF/Cassini will use CCDs similar to the ISS CCDs. The CRAF/Cassini spacecraft will be built and managed by JPL. The Space Telescope Imaging Spectrometer (STIS), a second generation ST camera, will utilize Tektronix CCDs. Originally the mission was to use two large 2048 x 2048, 21-micron pixel Tektronix three-phase backside illuminated CCDs. However, recent budget cuts have reduced the instruments capability to a single 1024 x 1024 pixel Tektronix device. The instrument and CCD are being developed at Ball Aerospace. The Multi-angle Imaging Spectra Radiometer (MISR) cameras will be based on a number of linear Loral CCDs. MISR is

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an earth observing system consisting of nine cameras to study earth's upper atmosphere. The Cosmic Unresolved X-ray Background with CCDs (CUBIC) camera will use a 1024 x 1024, 18-micron pixel Loral CCD to study background radiation of the universe in the x-ray. Many other NASA CCD imaging missions are in the proposal stage.

Paper Contents

This paper is divided into eight major chapters: (1) Introduction, (2) CCD theory and Operation, (3) Array and Pixel Size, (4) *Quantum Efficiency (QE)*, (5) *Quantum Yield (QY)*, (6) *Charge Collection Efficiency (CCE)*, (7) *Charge Transfer Efficiency (CTE)*, (8) *Read Noise*, and (9) *Frontside Pinning*, and (10) CCD Manufacturers and Foundries. We first begin in Chapter 2 with a brief discussion on solid state theory, operation, and basic architecture of the scientific CCD to aid in the discussion of subsequent chapters. In Chapter 3 limitations on CCD array and pixel size will be reviewed. It is in this area of development that the CCD has made its greatest strides. For example, the first commercially available area array CCDs fabricated by Fairchild nearly two decades ago contained 10,000 pixels (i.e., 100 x 100 pixel format). Today CCD arrays with over 16 million pixels (4096 x 4096 pixels) on a single chip can be procured - a factor of 1677 times more pixels than the original Fairchild CCD. There is no fundamental reason why the CCD can't continue to grow in size. Funding and interest are the main factors limiting CCD size currently. In Chapter 4 a discussion on QE performance and limitations for the CCD is addressed. QE performance has varied widely among CCD manufacturers and is the most inconsistent parameter of all CCD performance characteristics. The primary goal at CCD manufacturers has therefore been to develop a mature QE technology to achieve high, stable and consistent performance. Chapter 5 reviews the subject of quantum yield or the ability of the CCD to generate multiple e-h hole pairs per interacting photon or particle. This relatively new capability has opened numerous opportunities for the CCD. For example, CCD instruments referred to as *CCD radiation imaging spectrometers (CCD-RIS)* are used to precisely measure the energy of individual incident radiation events (e.g., photons and ions) and simultaneously image them. In Chapter 6 physical factors that limit CCE performance are discussed. In general CCE for the CCD is well-behaved and established. Sensors can be fabricated to achieve near theoretical performance in resolving spatial frequencies. However, future improvements are required to minimize charge loss internal to the CCD, an important CCE parameter that will be discussed. For example, CCD-RIS instruments are very vulnerable to charge loss mechanisms exhibited by the CCD. CTE, a very

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important CCD parameter, is discussed in Chapter 7. CTE has improved to levels that have exceeded everyone's expectation, essentially perfect, and is an area where future development is probably not required. Read noise, discussed in Chapter 7, has also been developed to near perfection. It is unlikely that new breakthroughs will significantly reduce the read noise of the CCD any further. However, we will report on an indirect noise reduction technique recently developed that lowers the noise floor to any level desired. Chapter 8 also discusses two important noise sources generated internal to the CCD. These are *dark current* generation, an unwanted source of charge that has been significantly reduced in the last two years, and *spurious charge* a source of charge generated when the CCD is clocked. In Chapter 9, miscellaneous but important characteristics about the CCD are discussed: *full well capacity*, *anti-blooming*, *high-speed erasure*, *residual image*, and *radiation damage tolerance*. These parameters can be controlled and optimized by a biasing technique referred to as frontside pinning. Chapter 10 presents a list of current scientific CCD manufacturers and foundries.

2. CCD THEORY AND OPERATION

The operation of a CCD is quite simple in principle. An elegant analogy thought up by Morley Blouke (Tektronix) and Jerome Kristian (Mt. Wilson Observatory) is often used to describe how it works. Imagine an array of buckets covering a field. After a rainstorm, the buckets are sent by conveyor belts to a metering station where the amount of water in each bucket is measured. Then a computer would take these data and display a picture of how much rain fell on each part of the field. In a CCD system the "raindrops" are the photons, the "buckets" the pixels, the "conveyor belts" the CCD shift registers and the "metering station" an *on-chip amplifier*.

Technically speaking the CCD must perform four tasks in generating an image. These functions are 1) charge generation, 2) charge collection, 3) charge transfer, and 4) charge detection. The first operation relies on a physical process known as the *photoelectric effect* - when photons or particles strikes certain materials free electrons are liberated. A brief discussion of this process associated with the CCD is given below. In the second step the photoelectrons are collected in the nearest discrete collecting sites or pixels. The collection sites are defined by an array of electrodes, called *gates*, formed on the CCD. The third operation, charge transfer, is accomplished by manipulating the voltage on the gates in a systematic way so the signal electrons move down the *vertical registers* from one pixel to the next in a conveyor-belt like

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fashion. At the end of each column is a *horizontal register* of pixels. This register collects a line at a time and then transports the charge packets in a serial manner to an on-chip amplifier. The final operating step, charge detection, is when individual charge packets are converted to an output voltage. The voltage for each pixel can be amplified off-chip and digitally encoded and stored in a computer to be reconstructed and displayed on a television monitor.

Photoelectric Effect

Silicon exhibits an energy gap of approximately 1.14 eV which is situated between the valence and the conduction energy bands. Incoming photons can interact with the silicon atoms and excite valence electrons into the conduction band creating electron-hole (e-h) pairs. The e-h pairs created are free to move and diffuse in the silicon lattice structure. The average lifetime for the carriers is on the order of 100 micro-sec or more when generated in quality silicon. After this time the e-h pair will recombine. Photons with energy of 1.1 to 5 eV generate single e-h pairs whereas photons with energy greater than 5 eV produce multiple e-h pairs. For example, at Lyman-alpha (1216 A or 10 eV), three e-h pairs are generated for each interacting photon on the average. Soft x-ray photons (100 eV - 10 keV) can generate hundreds or thousands of signal electrons making it possible for the CCD to detect single photons.

The useful photoelectric effect for silicon extends over a large spectral range (from 1.1 eV to 10 keV). This wavelength range covers the near infrared (NIR), visible, ultra-violet (UV), extreme ultra- violet (EUV), and soft x-ray. The cutoff for near IR photons (less than 1.1 eV) occurs because the photon does not have sufficient energy to elevate a valence band electron to the conduction band. Hence, the silicon is transparent to these photons and are not absorbed. For energies above 10 keV the probability of interaction is small, and the silicon atoms again look transparent to these incoming photons.

It should be mentioned that other optical materials can be used to broaden the spectral range of the CCD further. For example, *germanium CCDs* have been built at Loral which have delivered reasonable performance. Germanium exhibits a band gap of half that of silicon and therefore its IR response is good out to approximately 1.6-microns. In addition, since the density of germanium is greater than silicon, the x-ray response is extended out to about 20 keV.

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MIS Capacitor and Depletion

The fundamental building block of the CCD is the MIS capacitor mentioned above (refer to Figure 1). The MIS capacitor can be fabricated on *p*-type (boron doped) *epitaxial silicon* on which an insulator layer on the order of 1000 A is grown (composed of silicon dioxide or silicon dioxide and silicon nitride - a dual insulating system). This layer is followed by a conductive gate deposition (typically doped poly silicon). When a positive voltage is applied to the gate, majority carriers (holes) in the silicon are repelled from the region beneath the silicon-silicon dioxide ($Si-SiO_2$) interface leaving a depletion region. The potential variation within the depleted silicon is such that a *potential well* for electrons forms at the surface as shown in Figure 1.

The CCD is composed of an array of closely spaced MIS capacitors (3). There are numerous ways to arrange these capacitors to form a CCD imager. Conceptionally the simplest CCD is a three-phase device, the arrangement that Boyle and Smith used for their first CCD. In the three-phase device, a number of gates are arranged in parallel with every third gate connected to the same clock driver. The basic cell in the CCD, which corresponds to one pixel, consists of a triplet of these gates, each separately connected to phase 1, 2 and 3 clocks. If one now biases, for example, phase 1 high (say at 10 V) a depletion region forms and represents a region of higher electrostatic potential relative to the lower biased neighboring gates (say at 5 V). It is under this phase where signal electrons would collect in a pixel. The phase where charge collects is referred to as the *collecting phase* whereas the phases that are biased low are referred to as the *barrier phases* since they confine charge for the pixel on either side of the collecting phase.

A CCD area array imager can be thought of as many shift registers composed of many pixel elements. The image-forming section of the CCD is covered with closely spaced vertical registers or columns. The columns are separated by implanted potential barriers (called *channel-stops*) which prevent the spread of the signal charge from one column into the other. Channel-stops are highly doped boron p-regions which are held at ground potential (i.e., zero volts). Photoelectrons generated in these regions migrate and diffuse to the nearest potential well of a pixel (i.e., the collecting phase). The vertical columns are subdivided into pixels in the manner described above, by a series of conductive parallel gates that run perpendicular to the channel stops. Each line of pixels (i.e., one pixel per column) is controlled by one set of these vertical gates. A picture is read out of a CCD by a succession of shifts through the vertical

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registers. At each shift of the vertical section the last line of pixels transfers into a horizontal register. This register is also a CCD channel oriented at right angles to the vertical channels situated at the top and/or bottom of the device. Then, before the next line is shifted, the charge in the horizontal register is transferred to an on-chip output amplifier where charge for each pixel is converted to an output voltage. The *sensitivity* of the amplifier is expressed in volts per electron (approximately 1 to 4 micro-volts/electron is exhibited for most scientific CCDs). The device is then serially readout line by line, pixel-by-pixel, representing the scene of photons incident on the device.

Buried Channel Operation

The above discussion described a *surface channel CCD*, since charge packets are stored and transferred along the surface of the semiconductor (i.e., at the Si-SiO_2 interface). A major problem exists with surface channel CCDs since charge can become trapped in *interface traps* found at the surface severely limiting CTE performance (4, 5, 6). The first surface channel CCDs fabricated exhibited CTEs of 0.98 (i.e., 98 % efficient per phase transfer), much too low for scientific work. Although different attempts have been made to passivate and reduce the density of interface states through various process schemes, it became clear early on that surface channel operation could not be used for scientific CCDs especially when small charge packets are transferred. In addition, large area arrays to be developed required thousands of transfers demanding ultra-high performance, CTEs than surface channel sensors could never achieve.

To circumvent the surface state trapping problem and significantly improve CTE performance the *buried channel CCD* was proposed (7, 8, 9, 10). In a buried channel device charge packets are confined to a channel that lies beneath the surface "buried" in the silicon. In contrast to surface channel operation, the CTE for buried channel CCDs is amazingly high. As we will demonstrate in Chapter 7, efficiencies of greater than 99.999 % per *pixel transfer* are routinely achieved for buried channel CCDs fabricated today.

Figure 2 presents a cross-sectional view of a buried channel CCD showing a region of n-type material (typically a phosphorus implant) forming the buried channel. In comparison to a surface channel structure, the extra n-dopant reshapes the potential well so that electrons are forced to collect below the Si-SiO_2 interface. Two potential wells are shown for applied gate voltages of -8 V and 3 V. As with surface channel devices photoelectrons migrate to the highest potential seen a region

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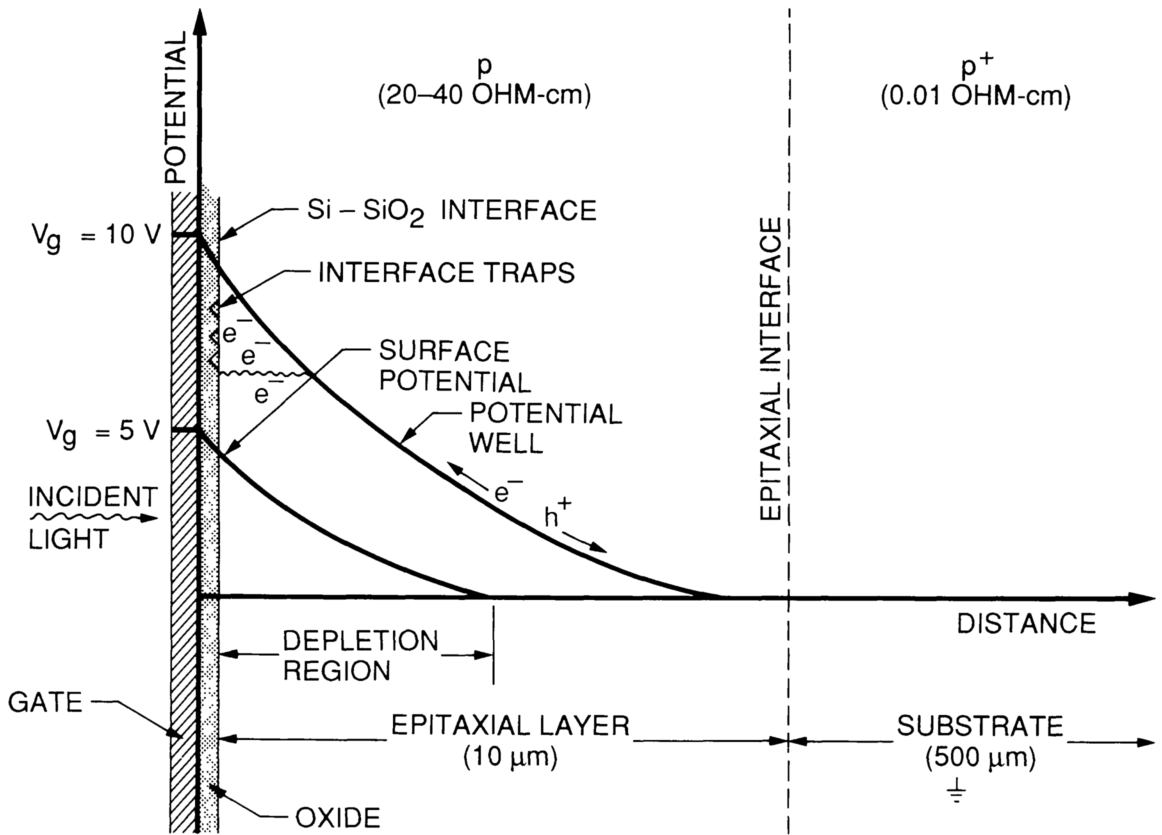

Figure 1. Surface Channel MIS Potential Well

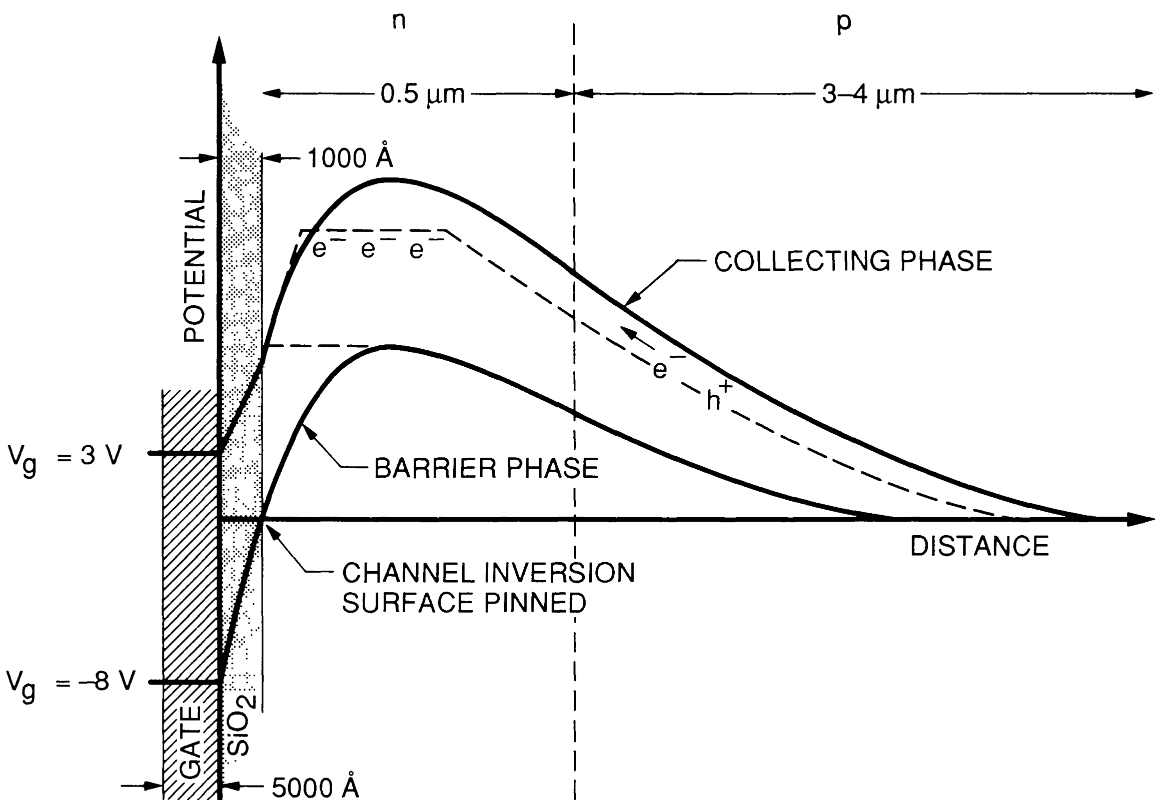

Figure 2. Buried Channel MIS Potential Well

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which is now situated between the $Si\text{-}SiO_2$ interface and n-p junction. If the gate voltage is changed from -8 to 3 V, electrons will leave the -8 V well and collect within the 3 V well. Photogenerated holes leave the silicon through the substrate contact which is referenced to ground potential (i.e., 0 V).

The potential well of a buried channel structure changes shape when signal electrons fill it (refer to the dotted potential well shown in Figure 2). Three important changes occur. First, the potential maximum (or channel potential) of the collecting phase decreases as it approaches the potential of the barrier phases. Second, the potential maximum of the well shifts towards the surface. Third, the potential well flattens and broadens as shown. When the potential of the collecting and barrier phases become equivalent charge will spill over the barrier phases into neighboring pixels. This example of charge spreading among pixels is referred to as *blooming* and is when the device has reached a condition referred to as *bloomed full well*. Another mechanism of charge spreading is when charge first interacts with the surface first before blooming. This state occurs when the potential maximum of the collecting phase equals its surface potential. This full well condition is referred to as *surface full well*. Chapter 9 discusses how the CCD can be biased into either state and also describes how optimum full well can be achieved.

Inversion and Pinning

A particularly important condition develops when a phase is driven negatively such that the surface and substrate potentials become equal (this state is shown for the barrier phase in Figure 2). Under this bias condition the n-channel at the $Si\text{-}SiO_2$ interface *inverts*, that is, holes from the channel-stops are attracted and collect at the surface. Reducing the gate voltage further generates more holes *pinning* and maintaining a surface potential of zero volts. The thin layer of holes at the surface is conductive and shields the silicon layer from the gate potential fixing the potential well shape (when inverted any change in gate bias goes directly across the gate insulator). Frontside pinning or *channel inversion* has a profound effect on CCD performance as we will discuss in Chapters 8 and 9.

3. AREA ARRAY AND PIXEL SIZE

Early Developments

It was recognized early in the development of the scientific CCD

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that the number of pixels required for most scientific imaging applications would be significantly greater than standard formats employed in commercial broadcast TV cameras (i.e., 320 (H) x 512 (V) pixels). Vidicon tubes developed and utilized for recent JPL planetary imaging missions were based on 1024 x 1024 pixel formats (e.g., the Viking vidicons cameras sent to Mars) and therefore, early development would focus on obtaining pixel counts this large. At the time (1973) it was unknown how many pixels could be packed onto a single chip. As it turned out fabricating arrays with pixel counts this many was the most challenging aspect in the development of the scientific CCD. Curiously the demand and challenge for even larger arrays today still exists. For example, astronomers always prefer larger CCDs as their telescopes continue to grow in size.

CCD development at JPL initially involved three US manufacturers: RCA, Fairchild, and Texas Instruments (TI). Fairchild was a pioneer in developing the CCD fabricating high performance buried channel devices. The sensors exhibited read noise floors of less than 30 e- rms (root-mean-square) and CTE's better than 0.99995 per transfer, a remarkable achievement considering that the CCD was invented only a few years before (Boyle's and Smith's original CCDs were surface channel and exhibited CTEs of 98 %). Fairchild CCDs were even commercially available: a 1 x 500 pixel linear CCD array and a 100 x 100 pixel area CCD array were the first devices to be offered to the scientific community at a modest cost (11). These early devices were a tremendous benefit in getting the scientific CCD off the ground. At JPL several *slow-scan* CCD cameras were built around Fairchild CCDs for test purposes. These early CCDs were also the first sensors used behind small astronomical telescopes. For example, in 1974 a 100 x 100 pixel Fairchild CCD was used in conjunction with a 8-inch Celestron telescope which may have produced the first CCD astronomical images of the moon and planets (i.e., "first light" for the CCD). Unfortunately the architecture philosophy that Fairchild followed and continues to do so today (i.e., *interline transfer* (12)) was not optimized for scientific performance primarily in achieving high quantum efficiency, an important CCD parameter to be discussed in Chapter 4.

RCA took a different approach initially: a *full frame* and *backside illuminated* CCD (to be discussed below) which in theory would achieve the highest QE sensitivity possible. RCA was developing the largest CCD at the time, a 512 (V) x 320 (H) pixel frame transfer device (13). Unfortunately, early RCA CCDs were based on surface channel technology mentioned in Chapter 2. Hence, CTE performance for these early detectors was poor and the read noise high compared to Fairchild CCDs. Also both RCA and Fairchild were concentrating on commercial formats with limited

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spatial resolution, unsatisfactory for JPL and scientific needs. It became clear from these early studies that a special R & D effort was necessary to combine the best attributes of all CCD technologies known at the time. JPL then contracted Texas Instruments to work on a scientific sensor based on backside illumination, full frame, buried channel, with pixel counts equivalent to or greater that the vidicon tube. The effort between JPL and TI progressed for over a decade and is where many breakthroughs for the scientific CCD originated.

CCD Array Shorts and Opens

The main limitation on CCD array size is directly related to the number of gate shorts and opens that result during the fabrication of the sensor. Simply put, the larger the CCD the greater the probability the sensor will exhibit a short or open. These defects are usually caused by contamination, such as dust particles, that land on the CCD silicon wafers during processing. Contamination events are minimized by means of special filters that filter the air that circulates through the process laboratory. Large CCD arrays fabricated require at least a class 100 clean room environment (100 particles per cubic meter) or better. A few CCD manufacturers maintain class 1 clean rooms where human intervention is not allowed. In these labs CCDs are fabricated by robots the approach used by the Japanese at TIJ in fabricating the SXT sensor.

Several types of CCD shorts have been identified and investigated over the years. For example, shorts between clock phases is one common shorting problem (i.e., *inter-level short*), a serious problem related to early CCDs fabricated at TI when 3-phase aluminum gate technology was employed. A short between clock phases for these early CCDs usually resulted in a "hard short" which either destroyed the external CCD clock drivers or led to poor CTE behavior in the vicinity of the short. The functional yield was extremely low due to the shorting problem (< 0.5 %). However, a few sensors as large as 400 x 400 pixels were fabricated and were the first scientific CCDs successfully employed at astronomical observatories. For example, a 400 x 400 pixel rear illuminated aluminum gate CCD was the first sensor used in JPL's traveling CCD camera system employed at Mt. Lemmon in Arizona on the Catalina 61-inch telescope.

The aluminum gate shorting problem experienced at TI was recognized as a serious problem which would limit array sizes to no larger than 512 x 512 pixels. In addition, the reliability of the aluminum gate CCD was questionable because *latent failure shorts* were often observed (shorts that would appear with use of the device), an important concern when the sensor is used in

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space applications. To circumvent the aluminum gate shorting problem TI changed to a *poly silicon gate technology* (14, 15) already successfully implemented by Fairchild and RCA (it appears that these groups were ahead of TI in this area of development at the time). Since doped poly silicon was significantly less conductive than aluminum an inter-electrode short was not catastrophic to drive electronics and global CTE performance. Poly silicon also had the advantage of being relatively transparent to incoming photons allowing for frontside illumination whereas aluminum gates were opaque requiring the CCD to be thinned and backside illuminated. The device yield at TI significantly improved when poly silicon gate 512 x 512 pixel CCDs were fabricated. The technology eventually led to 800 x 800 pixel versions, devices currently used by Space Telescope. Today nearly all scientific CCDs are based on poly silicon electrodes.

Another type of short that plagued early CCD development was the *substrate short*. A substrate short of any magnitude inevitably manifests itself as a *column blemish* induced by leakage current injected from the conductive gate into the signal carrying channel of the device. In fact, the majority of devices with substrate shorts would saturate the CCD due to the excessive leakage channel currents. The substrate short also impacted device yield at TI. For example, less than 2 percent of the WF/PC I CCDs passed the shorts test due in part to the substrate short. For this reason 114 lots of sensors were fabricated to satisfy WF/PC's needs (a WF/PC I lot contained 132 devices).

Triple polysilicon gate processing, used in fabricating three-phase CCDs is a high yield technology and has permitted large area array CCDs to be realized. Two-level poly gate processing is used in making two and four-phase CCDs and are easier to make requiring less process steps than three-level poly. However, this CCD technology has one serious draw back, the *intra-level short*. An intra-level short is produced during fabrication when a "bridge" of poly forms between the same poly level deposited (referred to as *poly stringers*). The poly bridge may be caused by a speck of dust that lands on the CCD wafer during processing preventing the poly layer to be etched properly. For example, four-phase CCDs that employ double poly typically utilize the first poly level for phases 1 and 3 and the second poly level for phases 2 and 4. An intra-level short that occurs in the first level would short phases 1 and 3 resulting in poor CTE for the entire line and for all lines above the troubled site (this type of CCD blemish is referred to as a *line drop-out*). Triple poly gate processing eliminates this difficulty since each level is intentionally connected and bussed together forming phases 1, 2 and 3.

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LOCOS Process

Fortunately advanced silicon processing techniques were also being developed at the same time the scientific CCD was evolving. These advancements were prompted by serious competition among silicon manufacturers world wide who were fabricating logic chips for computer related hardware (e.g., RAMS, DRAMs, micro-processors chips, etc.). These important advancements had an major impact on yield when CCD manufacturers utilized the same process recipes. For example, localized oxidation of silicon (*LOCOS*, a process developed at Phillips Laboratory) was optimized for CCD fabrication. The LOCOS process is based on the fact that silicon nitride can be used as a mask against thermal oxidation which becomes highly advantageous when fabricating CCDs. In addition, there are certain enchants (e.g., H_3PO_4) that removes silicon nitride but not silicon dioxide and vica-versa. In the LOCOS process the CCDs insulator is based on a dual insulator system (e.g., typically 500 A of silicon dioxide and 500 A of silicon nitride). This insulating system significantly reduced the number of substrate shorts compared to a single layer of oxide (1000 A) used initially by CCD manufacturers. Today most large area array CCD manufacturers use an oxide/nitride insulator. A few CCD manufacturers use a simple oxide insulator, however, device yields are typically lower with exception of those groups who benefit from ultra-clean facilities (i.e., class 1). The WF/PC I TI 3PCCD was built in a research laboratory (i.e., class 100) using a simple gate oxide layer, however, as indicated above tens of thousands of devices had to be fabricated to obtain a couple hundred good chips.

A common array size commercially available today is the 1024 x 1024 pixel CCD. The current yield for this array size is exceptionally high as demonstrated by several CCD manufacturers (TI, Tektronix, Loral, Kodak, Thomson, and GEC). For example, recent 1024 x 1024 CRAF/Cassini 12-micron pixel CCD lots using the LOCOS process exhibit a *shorts yield* as high as 75 % (i.e., 75 % of the CCDs don't show shorts) and a *cosmetic yield* without column blemishes as high as 25 % being achieved - an amazing accomplishment in contrast to early CCD lots built at TI a few years before. Even higher yields have been obtained for the new WF/PC II 800 x 800 15-micron CCD made at Loral.

Ultra-large CCD Arrays

CCD technology and fabrication is pushed hard when array sizes of 4 million pixels per array or greater are made. The difficulty is most apparent in the price-tag to the consumer. Although the price of the CCD as a whole increases dramatically as size increases, the cost per pixel is nearly the same. For example,

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the current cost for a thinned backside illuminated and frontside illuminated Grade 1 Tektronix 512 x 512 pixel CCDs is $6000 and $1800 respectively (2.29 and 0.69 cents per pixel). Similar devices based on a 1024 x 1024 pixel format are $35,000 and $25,000 (3.34 and 2.38 cents per pixel). Still larger, the Tektronix 2048 x 2048 pixel CCDs cost $110,000 and $53,000 (2.62 and 1.26 cents per pixel). The Tektronix CCD family is based on a 21-micron pixel.

The 4096 x 4096, 7.5-micron pixel CCD fabricated at Loral is the largest CCD fabricated in terms of pixel count (compare this CCD to Bell Labs first CCD which was only 8 pixels long (16)). The chip is the first CCD fabricated that can compete with the resolution capability of photographic film. The resolution power of the CCD is awesome. For example, two football fields set side-by-side can be resolved to 1 inch per pixel including the side and goal zones. Looking skyward, the 4096 x 4096 pixel sensor can cover 68 arc minutes of the sky with 1 arc sec resolution (the moon extends about 32 arc-minutes). The cost of the CCD is approximately $60,000 demonstrating the difficulty in fabrication of the device.

Tektronix fabricates the largest CCD physically, a 2048 x 2048, 21-micron pixel device occupying a single four-inch silicon wafer. Comparing the cost of the Tektronix chip to Loral's 4096 x 4096 pixel CCD it appears that they are about equally difficult to fabricate. Although the Loral CCD occupies less real estate than the Tektronix CCD the device has more pixels per unit area, a factor that also lowers device yield.

Based on todays CCD technology and yield figures it appears possible that a 8192 x 8192, 7.5-micron pixel CCD could be fabricated. This assumes that funding could be found in fabricating such a hypothetical device. The cost of the CCD would be significant since only one or possibly two devices from a lot run might be obtained (the cost of a CCD lot run ranges between $60,000 to $120,000 depending on the CCD foundry). However, a device this large would present numerous difficulties for the user, primarily in the area of data storage. The sensor would produce, for example, over 130 million bytes of information per image assuming 16-bit encoding. Such an enormous amount of data is equivalent to a 27 million-word book or about 250 encyclopedias. The sensor format would match that of four-hundred and nine 320 x 512 pixel CCDs. Readout time of the CCD would also present a problem. Assuming a single on-chip amplifier operating a 25 k pixels/sec, the device would require 42 minutes for readout. There are no immediate plans by any CCD group to fabricate such a device in the near future.

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A trick in beating the yield problem and obtain ultra-large CCDs is to mosaic them. Several CCD groups are currently using this approach. For example, Loral fabricates four 2048 x 2048, 15-micron pixel CCDs on a four-inch wafer. The sensors are designed so that non-shorted devices can be diced, butted, and mosaiced on two edges that can be organized into a 4096 x 4096 pixel format. Packaging costs are high when using this approach since very tight tolerances are required in butting the chips in keeping the seam regions between each device to a minimum (a couple pixels can be achieved). For similar packaging efforts it may be more cost effective to fabricate a full wafer CCD rather than resorting to mosaicking.

Silicon Wafers

A lot run of 2048 x 2048, 15-micron Loral CCDs consists of twenty-two 4-inch wafers yielding 88 devices. Higher yields could be achieved if larger silicon wafers were utilized. Although six-inch wafers are commonly used at leading US micro-electronic chip manufacturers who fabricate micro-processor and memory chips, wafers this size are not popular with American CCD manufacturers. Japanese groups utilize six-inch CCD lines primarily to satisfy the high commercial demands for video and still CCD camera markets. The 1024 x 1024 pixel SXT CCD was fabricated using six-inch wafers at Texas Instruments of Japan (TIJ). The yield for the SXT CCD increased significantly compared to the same CCD fabricated on four-inch wafers at TI in Dallas (TID).

Converting from a four-inch to a six-inch CCD line is an expensive investment involving five to ten million dollars for new processing gear (furnaces, implanters, reticle steppers, deposition systems, facilities, etc.). Unfortunately, the motivation and funds for such equipment to fabricate scientific CCDs isn't evident in the states. Interestingly CCD manufacturers may be forced into a six process since quality four-inch silicon may be in short supply in the future (currently six-inch material is easier to obtain than 4-inch). This is because non-CCD manufactures have been motivated to use larger wafers to remain competitive for yield and profit reasons. Experimental twelve-inch silicon wafers have even been grown implying that the demand for even larger wafers is on-going. It appears that US CCD groups will be required to keep up with these technology trends if the scientific CCD is to survive. It is important to note that the Space Telescope TI 3PCCD was built on 3-inch silicon wafers, material that is virtually nonexistent today.

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Pixel Size

Photolithography processes used in fabricating CCDs requires the precise position of a number of doped regions and interconnection patterns. These regions include implants and diffusions, contact cuts for gates, metallization and protective cover layers through which connections can be made to bonding pads. Typically seven to ten major lithographic steps using *reticles* or *masks* are required for each silicon wafer processed. For example, a basic three-phase CCD requires the following mask set: (1) field oxide (the mask that defines CCD channel and channel stops), (2) poly-1, (3) poly-2, 4) poly-3, (5) n+ mask (used in defining the source and drain regions for the reset and on-chip amplifier, (6) contact (mask that cuts oxide to make contact to poly electrodes, (7) metal (aluminum busses that contact to poly and n+ diffusions), and (8) bond pads. There are also several optional masks that can be selected depending on application.

A mask set is designed by a CCD designer using a Computer Aided Design (CAD) terminal. For example, the 1024 x 1024 pixel CRAF/Cassini CCD was designed with AUTOCAD 10, a CAD software package developed for personal computers (PC). Next the CCD design is sent to a specialty house where a computer converts the layout and directs an electron-beam to write the CCD pattern onto aluminized glass substrates producing the mask set. Mask sets can be obtained in fairly short order, a couple weeks is typical.

There are basically two types of mask sets used in fabricating CCDs referred to as (1) *contact* and *off-contact masks*, and (2) *projection masks*. In contact printing the mask is in intimate contact with the silicon wafer. With an off-contact reticle there is a space a few microns between the mask and wafer (the space significantly extends the life time of the mask). Projection printing uses an expensive optical system to project the image of the mask onto the silicon at a distance. Contact printing can achieve CCD design features of about 1-micron. Stepper masks can hold design features to about 0.2 microns, and therefore, are used when small pixel sensors are fabricated. Three-phase pixels as small as 5-microns square have been fabricated, the present limit at Loral for example.

One of the largest CCD pixels fabricated was a 52-micron square pixel designed by EG&G Reticon for JPL's High Resolution Imaging Spectrometer (HIRIS) CCD camera. The HIRIS pixel was based on a four-phase design providing 13-microns per phase. Although larger pixels were desired by HIRIS, a 52-micron pixel was felt to be the largest feasible without resorting to additional phases per pixel to transfer charge properly (64-phase CCDs have been fabricated for this purpose to achieve ultra-large well

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capacities with good CTE). Pixels are limited to the HIRIS size because the potential variation beneath the phases is for the most part uniform. Hence, there are no electric fields in the middle of the phase to transfer charge from phase-to-phase as the CCD is clocked. Charge primarily moves in a CCD because of *fringing fields* generated by neighboring phases (17, 18). Without fringing fields charge would sit beneath a phase and would only slowly transfer by diffusion and self-repulsion field effects (refer to Chapter 7). Fringing fields from adjacent phases extend into a phase only a few microns. Therefore, to achieve good CTE the length of a phase should be limited to about 10-microns or possibly longer depending on how fast charge is transferred. Measurements made on the first HIRIS CCD exhibited a horizontal CTE problem because the length of the last clocked gate (i.e., summing well) was designed too long and required nearly a micro-sec of transfer time to dump charge to the *output diode* or *sense node* (refer to Chapter 8). In that a pixel rate of 3 Mpixels/sec was required by HIRIS the summing gate was redesigned and shortened decreasing transfer time.

4. QUANTUM EFFICIENCY

This property of the CCD determines the sensitivity of the device to photons incident upon it, and of course, is a very important parameter in seeing very faint objects. Quantum efficiency basically measures photon loss and includes reflection loss at the surface of the sensor, loss by the absorption in the gate electrodes, loss in the gate insulator, loss of carriers via recombination in the silicon substrate, and for the near IR and x-ray radiation lack of sufficient photon absorption in the material on which the CCD is built. Several design and process approaches have been used to minimize these losses for the CCD.

In it's early development it was discovered that the CCD could achieve high QE over a very broad spectral range including the near IR (7000-11,000 A), the visible (4000-7000 A), the UV (1000-4000 A), the extreme UV (100-1000 A) and the soft x-ray (1-100 A). Such performance was first demonstrated by the thinned backside illuminated TI 3PCCD. Frontside illumination of the TI 3PCCD and other similar devices were limited to a small spectral range (the near IR, visible, and some of the x-ray spectrum). Limited coverage was due to photon absorption in the relatively thick gate electrodes. For example, at a wavelength of 4000 A, the absorption depth of a photon is only 2000 A in silicon (absorption depth is that distance where 63% of the incoming photons are absorbed, i.e., $\exp^{-1}$). Because the thickness of poly silicon gates are typically thicker than this (5000 A in the case of the TI 3PCCD) low QE was exhibited (a few percent at 4000 A).

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The gate absorption problem worsens in the UV and peaks mid-range at 2500 A where the absorption length is only 25 A (a few atomic layers) resulting in zero QE for the CCD. Reflection of photons from the surface is also the greatest at this wavelength, approximately 70 %. Shortward of 2500 A absorption and reflection loss decrease and the top layers of the CCD become less influential on QE. However, the frontside illuminated CCD only begins to show life in the soft x-ray (shortward of approximately 25 A) where photons can once again penetrate through the gate electrodes into the active silicon.

At either end of QE response, in the near IR (11,000 A) and soft x-ray (1 A), the CCD looks transparent to incoming photons because the absorption length of the photon is much greater than the active thickness of the device. For example, a 1.06-micron photon penetrates several hundred microns in silicon resulting in a QE of a few tenths of a percent. A similar cut-off response is exhibited at the end of the soft x-ray regime (i.e., 1 A or 10 keV). QE performance can be improved in these spectral regions by making the active cross-section of the device thicker. *Deep depletion* or *high resistivity* CCDs are being fabricated for this purpose. These sensors are fabricated on high resistivity silicon which deepens the pixel potential wells thereby collecting photogenerated charge made deep in the CCD. For example, conventional CCDs employ 10 to 50 ohm-cm resistivity silicon resulting in depletion depths not more than 10-microns. Deep depletion CCDs on the other hand employ resistivities of 1000 ohm-cm or greater resulting in depths of tens of microns with a proportional increase in QE in the IR and soft x-ray.

Backside Thinning

As mentioned above, thinning and backside illuminating the CCD will deliver the highest QE possible. Thinning a CCD is a simple procedure to perform. In fabricating the Space Telescope CCD the following thinning recipe was used at TI. Following wafer fabrication and die separation, a chip was mounted frontside down onto a 3-inch sapphire wafer. Then the active area on the backside of the chip was carefully masked using a hard wax. The sapphire disc and CCD were then mounted onto a teflon disc about the size of a hockey puck. The puck was then lowered and immersed into a plastic drum containing acid etching solutions (hydrofluoric, nitric, and acetic acids) which in combination rapidly etches silicon (the sapphire wafer, wax, and teflon puck are immune to the acids). The drum, tilted at 45 degrees, was then rotated slowly at 30 rpm rate reversing directions every minute or so. The teflon puck freely rotated in the bottom of the drum in an opposite direction to drum rotation. The chip was thinned from an initial thickness of about 300-microns to a

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thickness of 8-microns in about an hours time. Thinning essentially stopped when the epitaxial interface was reached because the etch rate of silicon significantly diminishes when low-doped, high resistivity epitaxial material is encountered. For the TI 3PCCD this rate was approximately 100 times slower, and therefore, the epitaxial interface was used as an *etch stop*. After thinning, the CCD was carefully removed from the drum, puck, and sapphire disc and thoroughly washed before mounting in a package.

Thinning and subsequent packaging at TI was a delicate process to perform and heavily took it's toll on sensor yield initially where many good CCD imagers were lost. Nearly 1 decade of thinning work was performed at Texas Instruments (by a single individual) for the Space Telescope effort. Thinning yields at the end of the WF/PC program were perfected to the level where only a few sensors were lost to the process.

Two major problems were associated with the thinning technique implemented at TI. First, as the CCD was thinned eddy currents set-up in the thinning drum preferentially etched the corners of the CCD. The corners of the WF/PC CCDs are about 1-micron thinner than the center of the device due to this problem. This characteristic led to nonuniform QE sensitivity across the detector (for some WF/PC CCDs this amounted to global QE nonuniformities of greater than 500 %). Second, mechanical stresses about the active area developed causing the thinned membrane to warp typically in a concave manner (the warp was specified by JPL engineers as the *potato chip factor*). For some thinned devices the flatness varied as much as 100-microns due to this problem. This trait made it difficult to focus an image onto the CCD when employed in fast optical systems. Custom corrective optics were sometimes positioned in front of the CCD to correct the aberration (telescopes faster than f/5 required fixes like this). To make matters worse the shape of the membrane would change and buckle as the device was cooled making the surface a moving target.

Fortunately thinning problems experienced at TI for the most part have been eliminated today. For example, Tektronix supports and backs the frontside of the CCD with a thick ceramic header before thinning is performed. This method guarantees that the CCD will remain flat after thinning. Also Tektronix thins the entire silicon wafer resulting in uniform thickness and QE response for individual CCDs. It is interesting to note that after the Tek device is thinned it must be electrically bonded to the package. To accomplish this the sensor is spot thinned beneath the bond pads coming in from the backside of the device (necessary since the frontside is covered with a ceramic header). The CCD is then

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bonded using the "backside" of the bond pad - a cleaver trick to implement in practice.

Backside Accumulation

To complete the thinning task the backside surface must be treated or very low QE will be exhibited, considerably less than frontside QE. Immediately after thinning silicon oxidizes forming a *native oxide* layer approximately 20 A in thickness. Through a very complex process the native oxide growth causes the surface to charge positively. The positive voltage induced in the oxide layer creates a *backside depletion region* and a corresponding *backside potential well* in the silicon that attracts and collects photogenerated electrons (similar to the creation of a surface channel potential well described in Chapter 2). The signal electrons collected eventually recombine at the surface and do not reach the frontside. In addition to this problem the native oxide surface is very susceptible to charging effects. For example, signal charge will get trapped at the surface negating the positive oxide charge causing the backside well to shrink in size. This phenomenon leads to an increase in QE. Over time, depending on operating temperature, the trapped charge will recombine lowering the QE back to its original level. The native oxide surface is also very sensitive to environmental changes (humidity, smog, etc.) resulting in a QE that is unpredictable from day to day. *Quantum Efficiency Hysterisis* or *QEH* is a CCD term used to describe such behavior in CCDs. QEH was observed for all eight Space Telescope CCDs. Unfortunately the QEH problem was not discovered until the WF/PC I instrument was assembled and tested. The dilemma severely crippled the project for QE varied more than 500 % at selected wavelengths and exposure periods (such stability is to be compared to a 1 % long term photometric stability requirement specified by the Space Telescope science team). An explanation for why the QEH problem was found so late in the WF/PC effort and its solution are discussed below.

To achieve high and stable QE the backside of the CCD must be negatively charged to drive signal electrons towards the front surface where they can be collected, transferred and detected. Four backside CCD treatment approaches are currently utilized to provide the necessary backside repelling fields for high and stable QE performance. The first method referred to as *backside charging* involves supplying free electrons on the native oxide surface. One method employed to accomplish the charging effect is to use an intense UV light flood (1800-2500 A). The UV photons pass through the native oxide layer and are immediately absorbed by the silicon a few angstroms from the Si-SiO_2 interface. Some of the photogenerated electrons created by the

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UV photons have sufficient energy to escape to the back surface where they can reside creating a small surface voltage (a few tenths of a volt). The negative potential in turn attracts and *accumulates* a thin layer of holes (approximately 200 A depending on the doping of the epitaxial material) at the Si-SiO_2 interface. The gradient of holes generates an intense electric field in the silicon as high as 10^5 V/cm when the CCD is fully charged. If the field strength is high enough an *internal QE* of 100 % can be achieved at all wavelengths, an important backside state referred to as the as *QE-pinned* condition. For some QE-pinned CCDs the backside fields are so strong that an internal gain has been observed which generates multiple e-h pairs for each interacting photon in the UV.

Other techniques have been invented to backside charge the CCD such as *corona charging* (a high voltage discharge in front of the sensor), and *gas charging* a method that briefly exposes the CCD to an oxidizing gas such as chlorine or nitrogen monoxide gases both that promote negative surface charge buildup. The eight Space Telescope CCDs use a UV light flood while in earth orbit employing the sun as the source of UV light. The sun light is brought into the side of the instrument at right angles to the axis of the main mirror by a piece of hardware referred to as the *light pipe*. The light pipe was added to the WF/PC I cameras before launch to fix the QEH problem costing 5 million dollars.

The main drawback to backside charging is the charge induced will not persist for long periods of time unless the sensor is kept cold (it has been shown that sensors remain charged indefinitely at -95 C, WF/PC's nominal operating temperature). To circumvent this problem another backside treatment technique referred to as the *flash gate* can be used to permanently generate negative charge. This method is based on depositing a monolayer (i.e., 1-atom thick on the average) of a high work function metal onto the backside of the CCD. The metal causes silicon electrons to "tunnel" through the native oxide layer and generate a surface potential equal to the work function difference between the metal gate and silicon (a few tenths of volt). Gold, platinum, iridium, and nickel have been used to achieve the QE-pinned condition. Another important advantage of the flash gate over backside charging is that anti-reflection coatings can be deposited on top of the gate to reduce reflection loss. This backside configuration has yielded very high QEs greater than 90 % in the visible for the CCD.

Unfortunately the flash gate like backside charging is also limited and fails to maintain the QE-pinned state under high vacuum conditions. Through a complex surface process not fully understood, the vacuum environment promotes additional positive

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charge buildup in the native oxide layer negating the negative charge generated by the flash gate. This collapses the internal fields in the silicon resulting in a lower QE (the device becomes unpinned). To bypass this difficulty the *biased flash gate* was proposed. As the name implies, the backside metal gate is biased slightly negative to compensate for the positive charge induced under vacuum conditions. Because the potential on the gate can be controlled externally, the user can control the QE of the detector and also acts as an electronic shutter. For instance, when positively biased a backside depletion well forms and charge is swept towards the backside and lost as though a shutter was closed. When biased negatively carriers are forced to the frontside resulting in high QE. Of course the electronic shutter control described only works for wavelengths where the photon absorption depth is less than the backside potential well depth induced (i.e., applicable for blue and UV wavelengths). The second generation WF/PC II camera had planned to use the biased flash gate to bypass the need to UV flood the CCDs as required by WF/PC I. Instead WF/PC II has elected to use new frontside illuminated CCDs fabricated by Loral using phosphor coatings to achieve good blue and UV QE (see next section on phosphor coatings).

Although the original biased flash gate was based on a platinum gate other groups (e.g., Lick Observatory in collaboration with EG&G Reticon) are now using a gate material made of indium tin oxide (ITO). ITO has an interesting characteristic in that it is conductive but transparent. The Lick group uses about 80 A of ITO deposited on a base of Si-O which acts as an insulator. High QE's have been achieved with the ITO structure when biased negatively.

The forth and most popular accumulation approach at CCD manufacturers is to dope the backside of the CCD with a very concentrated but ultra-thin layer of boron. Some CCD groups using this method are Sarnoff Laboratory, Lincoln Laboratory, Thomson-CSF, and Tektronix. The boron implant provides a permanent hole layer that generates a similar field condition at the backside of the CCD as the three backside accumulation techniques discussed above. The approach is effective in obtaining high QEs in the visible and UV. For example, off-the-shelf Tektronix backside illuminated CCDs deliver QEs greater than 85 % when anti-reflection coatings are also used (a simple silicon nitride layer has been successfully employed by Tektronix for this purpose). The UV response for the same detector exhibits a UV QE as high as 35 % at 3000 A.

The backside of the CCD can be doped in diverse ways depending on the processing scheme used. For example, Tektronix dopes the

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surface using a low-energy boron implant beam. When implanting with energetic boron atoms radiation damage is induced at the backside since silicon atoms are displaced from the lattice structure. These displacements form trapping and recombination centers for signal electrons leading to poor QE. Therefore, to "activate" the dopant and anneal the damage the surface of the CCD must be heated to a high temperature. When heating the vacancies recombine with interstitials restoring the lattice structure. The heating process must be selective for the device must not get too high or the aluminum bus lines and bond pads on the frontside of the CCD will evaporate. Only the immediate backside surface must be heated. This has been accomplished by using a scanning high energy pulsed laser beam or rapid surface annealers.

Sarnoff Laboratory follows a backside accumulation technique developed by RCA two decades ago. Unlike TI, Sarnoff thins the entire wafer before the aluminum bus lines and bond pads are deposited. A thick border of silicon around the perimeter of the wafer is left for handling purposes to finish the device. After thinning, the wafers receive a boron implant to provide the necessary accumulation layer as described above. The wafers are then sent back to the process line where they're placed into a furnace and heated to activate the boron implant. After annealing, the backside of the wafers are backed with a thick supporting glass. The CCD wafers then move on for aluminum deposition and later are diced, bonded and packaged. As demonstrated by Sarnoff, the technique also achieves high QE at the same levels as Tektronix when anti-reflection coatings are also employed. For extended UV response the glass support used by Sarnoff must be thinned away to expose the bare silicon surface, a process not required by Tektronix since the supporting structure is located on the frontside of the CCD.

Although the backside boron implant technique has demonstrated high QEs in the visible and UV, the QE-pinned state (i.e., 100 % internal QE) has not been fully realized over the entire photon spectrum. QE-pinned performance is crucial for radiation imaging spectrometers where the charge generated must be totally collected without loss and measured to assess incident energy (refer to Chapter 6 on quantum yield). Backside charging has demonstrated good performance in this area promoting strong internal electric fields with a minimum backside dead layer.

Phosphor Coatings

From the discussion above it can be seen that backside processing can significantly add to the cost of fabricating a CCD. An alternative and relatively straightforward approach used to avoid

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thinning and accumulation is to vacuum deposit an organic phosphor coating on the frontside of the CCD to convert incident UV photons into longer wavelength photons. The secondary photons produced penetrate beyond the gate electrodes into the active silicon achieving relatively good QE performance. Several different types of phosphors are being used. For example, WF/PC I CCDs are coated with a *coronene* phosphor that absorbs UV photons shortward of 3900 A and emits new photons at 5200 A. The coronene layer has one significant draw-back in that a "QE notch" is exhibited between 3900 and 4200 A, wavelengths where coronene is not sensitive. Although the WF/PC II CCDs are backside illuminated devices the coronene layer was required because the sensors exhibited very poor UV QE since the devices were not properly backside accumulated (for reasons unknown at the time).

Interestingly coronene was directly responsible for hiding the QEH problem that plagued the WF/PC I cameras discussed above. The coronene layer was inspected at TI and JPL using a UV EPROM lamp. Inspection was required to verify that the coronene layer was intact. For example, the CCD window for some flight sensors were contaminated with coronene because of an improper temperature vacuum bake-out cycle of the sensor package. Therefore, each time a CCD was inspected it became backside charged from the UV light exposure. Subsequent characterization and screening of the devices at JPL didn't show QEH traits since the CCDs were unknowingly backside accumulated by the UV light. The backside charge persisted for several weeks under room temperature and argon gas conditions (the WF/PC I CCD package was back-filled with an inert argon gas). Only when the CCDs were allowed to discharge over a long period of time did QEH traits become conspicuous. QEH revealed itself for the first time when the flight WF/PC I cameras were powered and tested. If the coronene layer had not been utilized there would have been no reason to expose the CCDs to UV light. QEH would have then been detected when the CCDs first arrived and tested at JPL.

The QE notch exhibited by coronene can be eliminated by using a different phosphor coating referred to as *lumigen* (a phosphor coating first developed by Photometrics). Curiously lumigen is the same constituent used in commercial yellow phosphorescence "high-lighting" pens. The lumigen layer is thermally vacuum deposited at 10^{-6} torr with the CCD at 80 C to a thickness of approximately 6800 A. Lumigen absorbs throughout the UV and some of the EUV (i.e., 500 to 4200 A) achieving a 100 % quantum yield emitting yellow/green photons at approximately 5300 A. QE's of 12-16 % have been achieved by the new WF/PC II lumigen coated frontside illuminated CCDs that cover a spectral range of 1200 to 4200 A. Lumigen is transparent in the visible and near IR and does not significantly influence QE performance is this region

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(QE is actually higher since lumigen does act as an anti-reflection coating). Thicker layers of lumigen (or coronene) will extend the sensor's response further into the EUV (i.e., shortward of 500 A).

The main difficulty with phosphor coatings is they have a tendency to evaporate under high vacuum conditions. For example, at 10^{-6} torr and a operating temperature above 60 C, lumigen will slowly evaporate from the CCD. The CRAF/Cassini CCD will circumvent this problem by packaging the coated sensor in a hermetically sealed package and back-filling with an inert argon gas to a half atmosphere. This configuration in conjunction with a quartz window will achieve a flat QE of 15 % from 1800 A to 4200 A under space vacuum conditions (approximately 10^{-6} torr) and an operating temperature as high as 100 C. The new WF/PC II CCDs have been sealed with a magnesium fluoride package window to achieve the same QE level but to Lyman-alpha (1216 A).

Two other problems with phosphor coatings should also be noted. First, coated frontside illuminated CCDs exhibit a slight reduction in MTF response (refer to Chapter 6) in the UV. This characteristic is because light that is generated by the lumigen layer will scatter from the target pixel into neighboring ones. Therefore, to minimize light scattering the frontside top layers (i.e., poly gates and oxide overcoat layers) should be fabricated as thin as possible to keep the phosphor in close proximity to the active silicon. This particular problem is not as concerning for backside illuminated CCDs since the phosphor is essentially in direct contact with the silicon (separated by a native oxide layer). Second, phosphor coatings only emit one visible photon per interacting photon, and therefore, multiple e-h pair generation is not possible when phosphors are used. Phosphor coated devices, for example, are not used in CCD radiation imaging spectrometers.

Frontside Illuminated CCDs

Different CCD technologies have been invented to bypass thinning and phosphor coatings to achieve relatively high frontside QE in the UV. Virtual-phase technology has been successfully implemented at Texas Instruments for this purpose. In virtual-phase a four-step potential profile within each pixel is implemented with ion-implantation, and a single overlying gate clocks two of these potential steps to effect charge transfer (the region of the pixel which is clocked is referred to as the *clocked region* and the region without the poly gate is referred to as the *virtual region*). Since there is only one poly gate layer that overlies half of each pixel, it is possible to achieve good short-wavelength response with frontside illumination. For example,

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the Galileo VPCCD achieves a 25 % QE at a wavelength of 4000 A, about a factor of five times higher than a Loral three-phase CCD. The virtual-phase device provides reasonable UV QE down to approximately 1800 A at which point the gate oxide and protective "scratch" oxide layer become opaque causing the QE to drop abruptly. The thickness of the oxide layers can be minimized in the virtual region to obtain improved UV and low-energy x-ray response as accomplished by the SXT CCD. For the SXT CCD the oxide thickness is less than 3000 A allowing x-ray energies of 500 eV and greater to be detected.

In many respects VPCCDs are more difficult to fabricate than multi-phase sensors. For example, fabricating a TI VPCCD requires at least 14 mask sets in patterning the levels for the device. In comparison, a simple four-phase CCD requires half that number. In addition, the various implants employed in a virtual-phase pixel must be critically aligned with sub-micron accuracy where multi-phase pixels do not require such precision. Currently TIJ is the only manufacturer that knows how to make virtual-phase CCDs.

In general, VPCCDs when utilized in low-signal applications exhibit relatively poor CTE performance compared to multi-phase CCDs. The difficulty has been traced to *spurious potential pockets* which trap charge in the signal channel because of improper potential well shape within the pixel defined by the implants. As mentioned above, alignment of the implants is crucial for this technology to work, and small misalignments often create potential pockets (or bumps) which trap charge. This problem was in part responsible for the need to fabricate 39 lots of VPCCDs for the Galileo effort to obtain the single CCD unit now in space. Single clock operation is an important feature that virtual-phase technology offers. Unfortunately, the inflexibility of this virtue has often proved to be a disadvantage for low-signal applications. Many CTE problems associated with multi-phase CCDs have been solved by manipulating the clock phases to collapse CTE pockets located in the signal channel (refer to Chapter 7). Many of the potential wells in a virtual-phase pixel are defined by implants not external gates, so the user cannot control them to achieve optimum CTE.

Open pinned-phase (*OPP*) CCD technology is similar to the virtual-phase CCD. An OPP CCD is constructed exactly as a three-phase CCD except that the third level of poly is not deposited leaving a portion of the pixel open to UV photons. In place of the third phase, two implants are incorporated. The first implant adds more phosphorus to the buried channel increasing the channel potential for signal charge to collect. The second implant, a concentrated but very shallow implant of boron, pins the surface

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potential at the Si-SiO_2 to substrate potential (the conductive layer is internally connected to the channel stops which are connected to ground). This implant is important to assure that the potential well beneath the open region remains fixed as phases 1 and 2 that neighbor the open-phase are clocked. Both implants are self-aligned by poly levels one and two. An OPP pixel is typically designed so that phases 1 & 2 occupy half the pixel whereas the open-phase occupies the other half. Other arrangements are possible depending on full well and QE performance desired. In OPP CCD technology only the vertical registers employ the open phase and two extra implants. The horizontal registers always include the third poly level since QE performance for this register is not important. Although a scientific OPP CCD has not been successfully fabricated several three-phase CCD groups are pursuing the idea to avoid thinning and phosphor coatings. The CUBIC CCD mentioned in the introduction is based on OPP technology.

An alternative approach to OPP is to deposit a ultra-thin conductive gate within the OPP region that can be clocked to avoid implants. Several gate materials are possible candidates. A straightforward processing approach is to deposit a thin layer of poly silicon. CUBIC CCDs will attempt to deposit gates as thin as a few hundred angstroms for this purpose.

Lastly we should mention that transparent gate electrodes can be used to achieve good frontside QE. For example, Kodak has developed a ITO gate electrode process which has yielded good blue and UV QE.

5. Quantum Yield

Quantum yield is defined as the number of e-h pairs generated per interacting photon or particle. Multiple electrons are generated for photons shortward of 3000 A. For photon energies greater than 10 eV (i.e., 1000 A) the quantum yield is simply equal to the energy of the photon (eV) divided by 3.65 eV/e-. Therefore, by measuring the charge generated of an interacting photon one can determine its energy through this relationship. Its energy can then be referenced back to the chemical element that liberated the photon initially (i.e., spectroscopy). CCD radiation imaging spectrometers (CCD-RIS) are used for this purpose and demand near perfect performance in read noise, CCE, and CTE, characteristics to be reviewed in Chapters 6, 7 and 8. The *energy resolution* or accuracy in which a CCD can measure the energy of a photon is highly dependent on these parameters.

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Fano-noise

As indicated above it takes 3.65 eV of energy on the average to produce a single e-h pair for energetic photons interacting with the CCD. If all the energy of the photon were used to produce e-h pairs directly, there would be no statistical variation in the amount of charge generated by the event. However, a finite amount of energy is transferred to the silicon lattice by non e-h processes (thermal), giving rise to a small statistical difference in the number of e-h pairs actually generated. This uncertainty is characterized by the *Fano-factor* originally formulated by U. Fano in 1947 to describe the uncertainty of the number of ion-pairs produced in a volume of gas following the absorption of ionizing radiation. *Fano-noise* (in rms e-) is given empirically by $(F \times S(e-))^{.5}$ where F is the Fano-factor (0.1) and S(e-) is the charge generated by a photon. For example, a 5.9 keV x-ray photon generates 1620 e- with a Fano-noise of 13 e- rms. For a CCD to exhibit *Fano-noise limited* performance its read noise must be less than the Fano-noise generated by the interacting photons. Note when the energy of the x-ray decreases the CCD read noise must also decrease for the sensor to remain Fano-noise limited. As discussed in Chapter 8, noise floors of 1 e- rms can be achieved allowing Fano-noise limited performance to cover the soft x-ray region and a part of the EUV spectrum.

Proton Radiation Imaging Spectrometers

Frontside illuminated CCDs have been recently calibrated to measure the energy of incident protons and other high energy ions. When protons, for example, pass through a CCD they leave an ionizing trail of e-h pairs as the proton interacts with silicon atom orbital electrons. The charge generated depends on the loss of energy deposited in the photoactive thickness of the CCD (i.e., the thickness of the epitaxial layer). For example, a 1 MeV proton has a *range* of 15.67 microns in silicon and deposits 500 keV of energy in the first 10-microns, a typical epitaxial thickness. The remaining 500 keV is deposited in the substrate of the sensor. The amount of charge collected by pixels is simply equal to this energy (500 keV) divided by 3.65 eV/e- yielding 137,000 e-. The charge generated by a 10 MeV proton in 10-microns is only 23,000 e- since its *stopping power* (energy deposited per unit distance) is less than a 1 MeV proton. A 10 MeV proton has a range of 697-microns in silicon. Less signal is generated for higher energy protons.

A *proton QY* curve (charge generated as a function of proton energy) for normal incident protons has been experimentally generated using a SXT TI VPCCD over an energy range of 50 keV to

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10 MeV (protons were supplied by Cal Tech's Van De Graff ion accelerator). A peak response in QY occurs at 800 keV where 210,000 e- per interacting proton is measured. For energies less than 800 keV the QY response falls because: (1) less charge is generated since proton energy is smaller, and (2) a significant portion of the protons energy is lost in the overlying frontside gate structures (the QY response drops to zero at 50 keV where the protons range is equal to the thickness of the oxide layer). The QY above 800 keV is measurable for proton energies up to about 1 GeV. However, above 50 MeV it becomes difficult for the CCD to discriminate between proton energies since the stopping power is nearly the same over a 10-micron region (e.g., a 100 MeV proton generates only 1.61 times more charge than a 200 MeV proton).

The limiting energy resolution (or *energy straggling*) for the CCD in theory should be limited by Fano-noise, however, measurements performed with the SXT sensor showed a much greater uncertainty. For these experiments the problem was traced back to Cal Tech's proton source where straggling energies of 30 to 70 keV (FWHM) were measured, significantly greater than Fano-noise. Future QY tests will therefore utilize a monoenergetic proton beam to measure the CCDs true energy resolution.

6. CHARGE COLLECTION EFFICIENCY (CCE)

The ability of the CCD to record and reproduce the spatial information in a scene is an important measure of the utility of the sensor. For the CCD, this means that all of the charge generated by scene photons incident on a given pixel should be collected by that pixel. Three phenomena influence the perceived charge collection ability of the CCD; two of these, *charge diffusion* and charge loss in the neutral substrate is natural and the other CTE is essentially an artifact. In the later case CTE influences the output signal in a manner that diverts charge from the target pixel to trailing pixels (referred to as *deferred charge*). Not all charge generated by the illumination at a given site is detected at the output amplifier when that pixel is read out. As we shall discuss in Chapter 7, current CCD fabrication technology can provide devices with CTEs as high as 0.9999995, and therefore, this effect can in most cases be ignored.

The most serious contribution to the degradation of CCE in CCDs is charge diffusion and *recombination loss*. In the photosensitive volume of a CCD there are essentially three regions that influence the charge collection process: (1) the depletion region, which includes the charge carrying channel and the depleted bulk beneath it (i.e., the CCD potential well), (2)

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an undepleted, *field-free* neutral bulk below this that extends roughly 5 to 15-microns for most scientific CCDs fabricated depending on the thickness of epitaxial layer, and (3) a region of high recombination that can be the surface of untreated backside illuminated CCDs, or low-lifetime substrate material in frontside illuminated devices (the diffusion length of a carrier generated in substrate material is approximately 10-microns compared to several hundred microns when in the epi layer). If charge is created within the depletion region associated with a given potential well, there is a high probability that all signal charge will be collected in that pixel. For charge generated within the undepleted, neutral bulk, there is a good probability that it may spread into surrounding pixels and exhibit recombination loss if generated far from the frontside depletion edge.

Frontside illuminated sensors built on epitaxial thicknesses equal to or less than the pixel size will usually achieve excellent spatial resolution for all wavelengths covered. However, sensors built on thick epitaxial silicon will show degraded performance for near IR wavelengths since these photons are absorbed deep in the CCD. Deep depletion CCDs discussed in Chapter 4 are fabricated to alleviate diffusion problems like this. Backside illuminated CCDs may also exhibit diffusion traits when exposed to blue and UV photons since the surface charge generated must usually diffuse through field free material before reaching the frontside depletion edge (frontside sensors won't experience this problem since blue and UV photons interact directly within the potential well).

In theory backside illuminated CCDs can achieve the highest CCE possible. This is because the thinned device allows field control over most of the photosensitive volume by eliminating neutral bulk material. Unfortunately the majority of backside illuminated CCDs fabricated exhibit poor CCE because they have not been sufficiently thinned to the frontside depletion region or the fields generated by the accumulation layer are too weak to direct charge to the frontside properly.

CCE Tests

Three tests are used to measure charge collection efficiency for the CCD: 1) *modulation transfer function (MTF)*, 2) *contrast transfer function (CTF)*, and 3) *x-ray* response. MTF and CTF characterize charge diffusion effects whereas the x-ray technique characterizes both diffusion and loss providing an absolute measurement of CCE. The MTF describes the ability of the device to respond to sinusoidal spatial modulations of the signal intensity as a function of the spatial frequency. Because the

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CCD is a discrete sampling device, the best MTF obtainable is 63% at *Nyquist frequency* (Nyquist frequency is defined by d/2, where d is the pixel spacing in units of mm. e.g., the Nyquist frequency for a 15-micron pixel CCD is 33.3 cycles/mm). The CTF measures the CCDs response to a square-wave spatial frequency. The maximum CTF that can be obtained at Nyquist is unity. CTF measurements are easier to perform than MTF since it is often difficult to find a stimulus that varies sinusoidally in intensity. CTF is typically measured using a black and white "*square-wave target*".

Measuring the MTF at Nyquist for a CCD is not a easy test to perform. Quite often MTF is not limited by the sensor but instead limited by the MTF of optical system or target utilized in the measurement. MTF is also governed by the ability of the user to adjust the focus of the target onto the CCD properly for each wavelength investigated. These problems (focus, target MTF, wavelength dependence, etc.) can be circumvented by measuring the sensor's *edge response*, a measurement of the contrast change of an abrupt dark-to-light transition. An edge response is performed by projecting an "knife edge" of light onto the CCD using a collimated light source without a lens. The knife edge (a thin piece of shim stock can be used) must be located as close as possible to the surface of the CCD to minimize diffraction and light scattering effects. Critical edge responses are performed by depositing a thin layer of aluminum directly on the surface of the CCD to guarantee a perfect dark-to-white transition (note that *frame transfer CCDs* include an aluminum light shield that can be used to measure the vertical edge response).

Perfect edge responses have been demonstrated by frontside illuminated sensors when stimulated with visible photons. Therefore a 100 % CTF at Nyquist is possible for the CCD (i.e., a white to black transition occurs in one pixel). The lack of a sharp transition is directly related to the ability of the signal charge to diffuse laterally from beneath the illuminated pixels to those that are not illuminated. Edge response data can be converted to MTF form through Fourier Transform if desired.

X-ray CCE

As mentioned in Chapter 5, soft x-ray photons have much higher energy than do visible light photons. Absorbed by silicon, this additional energy generates multiple e-h pairs in the CCD. In contrast to the visible light case, x-ray electrons are generated in a very small cloud diameter (less than 1-micron), essentially a perfect point source. An equivalent number of visible photons would generate e-h pairs throughout an appreciable width and thickness of the device, and their number could not be measured

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with an accuracy that is comparable to the uncertainty in charge created by a x-ray photon. The degree of charge loss and charge splitting experienced by an x-ray event depends upon where in the pixel the photon is absorbed. Photons that are absorbed within the frontside depletion region of a given pixel are typically seen as the ideal event and are called *single pixel events*. Photons that are absorbed below the depletion region, in the field free area of the CCD, create a charge cloud that thermally diffuses outward until reaching the sharply-defined potential wells at the lower boundary of the pixel array. At that point, the charge cloud may split beneath the *target pixel* into two or more packets, which are collected in adjacent pixels. Events of this type are called *split events*. Events where charge is not conserved have been simply named *partial events* and are usually generated in regions deep within the CCD where loss of carriers through recombination occurs common to the thick frontside illuminated CCD. X-rays can therefore be used to measure charge collection loss in an absolute sense.

As mentioned above MTF and CTF are test tools used to characterize charge diffusion effects in CCDs, however, absolute charge loss must also be included when measuring CCE performance. For example, a backside illuminated that is not properly accumulated can exhibit high MTF but poor CCE performance because charge may recombine at the backside surface. Charge loss in CCDs is critical to radiation imaging spectrometers. If charge is lost in the collection process the energy of the photon or particle will be underestimated. If charge diffuses among pixels the energy resolution of the device is reduced because the charge in the affected pixels must be summed increasing the read noise (noise would increase by the square-root of the number of pixels summed).

Although backside illuminated TI 3PCCDs have demonstrated excellent CCE performance in terms of charge diffusion and loss, in general the device performs worse than its frontside counterpart (due to thinning and accumulation inconsistencies). This characteristic is generally true for most backside illuminated devices fabricated today. For this reason most radiation imaging spectrometers proposed are based on frontside illuminated CCDs although absorption by the front gate structures severely limits their low-energy response. It is hopeful that virtual and OPP CCDs can be developed to solve CCE problems since these detectors can potentially yield the best performance by minimizing the dead layer above the open regions and allowing radiation events to directly interact with the frontside potential well.

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7. CHARGE TRANSFER EFFICIENCY (CTE)

The charge transfer efficiency is a measure of the ability of the device to transfer charge from one pixel to the next. This process for todays CCDs is amazingly efficient. Typically, for well-made buried channel devices, the CTE will be in the range of 0.99999 to 0.999999 for relatively high signal levels (1000 e-). Assuming a CTE of 0.999999, this means, that for a CCD of 1000 pixels on the side, 99.8 % of the charge will remain in the pixel farthest removed from the output after it has been transferred to the output (2000 pixel-transfers). The rest is lost through recombination or dribbles out as a deferred charge in trailing pixels.

Theoretically three primary mechanisms are responsible for charge transfer in a CCD: self induced drift (18, 19, 20), thermal diffusion (18, 20, 21), and a fringing field effect. The relative importance of each of these is primarily dependent on the charge packet size. Both thermal diffusion and fringing fields are important for transferring small amounts of charge whereas self-induced drift (caused by mutual electrostatic repulsion of the carriers within a packet) dominates charge transfer for large packets. Experience has shown for scientific CCDs operated slow scan (say less than 100 kpixels/sec) that the mechanisms listed above are only of secondary importance and that CTE is instead influenced by four other factors related to electron traps. These are, (1) *design trap*, (2) the *process trap*, (3) the *bulk trap*, and (4) the *radiation induced trap*.

Design Induced Traps

The first CTE trap to consider, the design induced trap, is the one about which is known the most. The trap is usually the result of a design feature that results in a small potential trap or barrier. This type of trap is typically characterized by a region in the device where the signal channel narrows and charge is forced to transfer from a wider region of the channel into or through a constriction. This in turn produces a potential barrier in the channel where small quantities of charge can be trapped.

The best known example of the design induced trap is related to Space Telescope's TI 3PCCD, although many other examples exist. When first characterizing the CCD, it was observed that each event in the array exhibited a small deferred charge tail in the vertical direction. The tails were roughly the same length from column to column and grew exponentially in length with lower operating temperatures and faster vertical clock rates. The CTE tails were low level, amounting to a few hundred to a couple

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thousand electrons depending on the device tested. Because the deferred tails observed were nearly the same length for each column measured, it was suspected that the transfer gate between the array and the horizontal register contained a trapping site. By trial and error, different clock voltages were applied to the transfer gate region in hopes of influencing CTE performance and thereby locating the trap. Many groups actively participated in finding a cause and solution to the dilemma because the sensitivity of the WF/PC I camera and its photometric accuracy would be in serious jeopardy. As it turned out the TI 3PCCDs and drive electronics were almost flown as is. The origin of the problem remained a mystery for nearly two years until x-ray characterization was invented and used to characterize CTE behavior in an absolute sense (a subject to be discussed below). Using x-rays it was discovered that if the negative level of the phase preceding the transfer gate (phase 1) was driven more negative during line transfer, that the absolute CTE improved significantly. The negative clock solution saved the day for Space Telescope and was immediately implemented into the instrument without delay.

In the design of the Space Telescope CCD, the channel-stop regions were made wider under half of the transfer gate to properly transfer charge into the horizontal register. Unfortunately, due to the small geometries involved, constricting the channel in this region caused a slight decrease in channel potential, creating a trap in front of the transfer gate. Driving phase 1 negatively caused the fringing fields from that phase to extend into the transfer gate thereby collapsing the trapping site. The more negative phase 1 was driven the smaller the trap and corresponding CTE improvement. In conjunction with driving phase 1 negatively it was also advantageous to leave the transfer gate in the high state as long as possible to allow trapped charge to thermally escape from the trap into the horizontal register during line transfer.

The phase-1 solution did not represent a total solution since a 50 to 200 e- charge loss remained in the transfer gate depending on the sensor tested. The remaining problem is not readily apparent in *flat fields* or extended object images since the trapping region is continuously supplied with charge during readout. However, the problem is apparent when low-level point source signals are imaged (e.g., star images). For example, a 50 e- charge packet is completely swallowed up when it passes through the transfer gate region being redistributed in many trailing pixels as deferred charge. For this reason the WF/PC I cameras introduce approximately 100 e- of optical *fat-zero* into the array before an exposure is taken. The fat-zero fills in the trapping region allowing signal charge to transfer through

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unimpeded. Unfortunately the introduction of 100 e- results in an increase in *shot noise* (by 10 e- rms).

Nearly 50,000 Space Telescope CCDs were fabricated before the transfer gate problem had been clearly identified. It is now clear that the trapping problem for the sensor could have been prevented if the CCD was designed differently. Today, CCDs are designed so that the signal carrying channel is constricted at the end or beginning of the transfer gate as opposed to midway in the phase as implemented by Space Telescope. Unfortunately the CCD used by Space Telescope was never redesigned and therefore the problem exists today for all sensors in use. Currently over 100 sensors are employed in ground based CCD cameras including the eight flight units aboard Space Telescope.

Processed Induced Traps

The second type of defect which can severely degrade CTE performance is the process induced trap. These traps can themselves be classified into two categories: those that are uniformly distributed along the signal channel and cause a global CTE effect (these are referred to as spurious potential pockets), and those that are randomly distributed and isolated to individual pixels (these are referred simply as *localized traps*).

Spurious potential pockets is a term used to describe loss of charge during charge transfer due to improper potential well shape and/or depth beneath the pixel. These effects, often due to poly silicon edge lifting, and boron lateral diffusion have been examined by many groups. Spurious potential pockets are relatively easy to identify since a fixed amount of charge is deferred for each pixel-transfer. The problem is more pronounced for large CCD imagers where many transfers are executed. For example, an x-ray event of 1620 e- will lose 1000 e- to spurious pockets over 1000 pixel-transfers assuming only 1 e- is lost in each transfer cycle.

The most serious CTE problem for the CCD is associated with the localized trap. The behavior of a localized trap is similar to the design induced trap discussed above. Defects like this affect CTE on a local, random level. Localized traps have been seen in devices from every manufacture reflecting a variety of differing fabrication technologies. They appear to be present in devices fabricated with both a simple oxide gate structure as well as devices fabricated with a oxide/nitride dielectric, although measurements tend to indicate that the magnitude and frequency of occurrences of these traps is more severe in devices with dual dielectric. These defects are present in devices fabricated in epitaxial as well as bulk material and are present

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independent of the starting resistivity of the p-substrate. To complicate the issue, the frequency of traps observed in an array varies significantly (from a few to hundreds for any given CCD) from lot to lot even though the same fabrication recipe is employed. The traps are capable of capturing a wide range of charge, from a few electrons to several hundred thousand electrons. The localized trap is usually confined to a single pixel, and detailed tests show them to be localized to a single level of poly-silicon within a pixel. In depth physical examination (e.g., SEM analysis) of the pixel in question has generally failed to yield a strong correlation between structured defects and pixels with traps. The presence of traps in a CCD is independent of the gate structure (1, 2, 3, and 4-phase CCDs all have exhibited the trap problem). The filling and emptying of these traps is strongly affected by the impressed clock voltage but don't appear to be dependent on edge speed.

Although the presence of a trap in a vertical column is undesirable, its occurrence in the horizontal register can make the CCD totally useless. The localized trap problem has severely taken its toll on sensor yield in the past at several CCD manufacturers. Currently for most localized traps observed their exact origin remains a mystery (the intra-level short described above is one exception since this type of trap is well known to two and four-phase CCD manufacturers), fortunately, the difficulty has been for the most part been solved via trial and error processing. However, on occasion a lot of CCDs is fabricated that exhibit isolated traps making the problem still unpredictable.

Bulk Traps

Bulk traps, are due to deep-level metallic impurities (such as gold, iron etc.) or lattice defects associated with the silicon material on which the CCD is built (22). Bulk traps that happen to lie within the charge transfer channel will trap charge typically involving a single electron. Bulk traps are generally not a problem for CTE performance since todays starting wafers and processes used to fabricate the CCD have improved enormously in the last few years. However, bulk traps determine the ultimate CTE that can be achieved by the CCD (i.e., CTE performance is *bulk state limited*). On occasion a particular bad lot of silicon wafers is used that exhibit a high density of bulk traps influencing CTE more than expected.

Two techniques are available to the user to improve CTE when bulk states become a problem. Bulk traps usually become active at low operating temperatures where the emission time constant of the traps become equal to the time in transferring charge from one

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phase to the next. To avoid the bulk trap problem the user can operate the CCD at warmer temperatures allowing trapped charge to escape more quickly during the transfer period. The second improvement will result by increasing the clock over-lap transfer period allowing more time for charge to escape from the traps. These two factors (operating temperature and transfer period) are varied extensively to optimize CTE performance for CCDs. Ultra-high CTEs have been achieved in this manner, 0.9999995 or greater, levels where CTE is extremely difficult to measure. It is interesting to compare this performance to the first CCDs tested twenty years ago (Refs. 1 and 2). Early Bell Lab CCDs exhibited CTE's of only 0.98, 40,000 times worse than achieved currently.

To avoid CTE surprises caused by bulk traps, new silicon wafers are screened before a full production run of CCDs is initiated. The screening process is accomplished by selecting a few sample wafers and including them in on-going CCD runs that use silicon already verified for good CTE behavior. The sample wafers are then tested and used in future lot runs if they past certain CTE criteria (these criteria will be discussed below).

Radiation Induced Traps

Radiation traps are induced in the signal channel by energetic particles and photons (e.g., protons, electrons, neutrons, heavy ions, gamma rays, etc.) that displace silicon atoms from the lattice structure. Silicon vacancies created by incident radiation are unstable and typically migrate to favorable positions in the lattice. Usually vacancies become trapped near impurity atoms due to the stress imposed on the lattice by the impurities. For buried channel CCDs doped with phosphorus, the formation of a phosphorus-vacancy (*P-V*) complex is favored. The activation energy for this type of defect is approximately 0.4 eV below the silicon conduction band/edge. P-V centers are similar to bulk traps for they also extract electrons from the signal channel.

Radiation damage is important characteristic to consider when CCDs are used in space where energetic particles and photons are found. The problem is becoming more critical as CCD arrays grow larger in size and CTE performance improves. For example, a relatively small *RAD* dose (a RAD is equivalent to 100 ergs of energy absorbed by 1 gram of silicon) of low-energy protons can significantly degrade CTE performance because of P-V traps induced, a dose that is readily experienced in space.

Several solutions for the bulk radiation problem have been

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devised and implemented. The most straightforward remedy employs an external shield that surrounds CCD protecting it from radiation events. Unfortunately, to be effective massive shields must be employed for space particles vary over a wide energy range. Protons, for example, vary from a few eV to over a billion eV making it practically impossible to shield all of them from the CCD. For instance, a 1-cm thick tantalum shield will only stop protons below 100 MeV. CRAF/Cassini, Galileo, and Space Telescope use 1-cm tantalum shields to maintain good CTE over the mission life times (10 years or more). However, the external shield translates into a 7 kg weight penalty for each CCD protected. AXAF is planning to use 75 pounds of external shielding to protect their CCDs. It is interesting to note that vidicon tubes flown on past JPL planetary missions are insensitive to radiation damage and spurious signals generated by radiation events. The weight advantage once advertized for the CCD over vidicon imagers is not as significant as once believed because of the additional shield weight required for radiation protection. Nevertheless, CCDs are more attractive than vidicons for many other reasons.

P-V traps exhibit a different activation energy and emission time constant than bulk states usually becoming active at warmer operating temperatures. A key solution to the radiation damage problem takes advantage of the characteristic by cooling the CCD to cold temperatures. When the CCD is cooled the radiation traps can be frozen out so when filled with electrons they will remain filled for very long time periods and not influence CTE performance. For example, P-V traps will freeze-out at -90 C even at slow-scan rates (<20 ms line times). An IR light flood is usually used in conjunction with cold operation to fill in the traps before an exposure is taken (this technique is used by Galileo and CRAF/Cassini). Cooling the CCD also has the advantage of freezing out radiation induced *dark spikes*, pixels that generate abnormally high levels of dark current because of radiation lattice damage (refer to Chapter 9 on full well capacity).

The design of the CCD can also be modified to help alleviate the radiation problem. For example, the *Notch CCD* design incorporates a small signal carrying channel built into the main channel to minimize charge interaction with radiation traps when transferring small charge packets. For example, CRAF/Cassini CCDs have been fabricated that use a 3-micron notch channel. The notch channel is formed by doping the main channel with additional phosphorus increasing the potential well depth in the region. Because the potential is higher, charge is confined to the notch channel and hence less traps are seen by the charge packet. Proton damaged CRAF/Cassini CCDs exhibited a horizontal

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CTE improvement of a factor of ten when a notch channel was employed. For these experimental CCDs a 3-micron notch was centered in the sensor's 40-micron horizontal channel. The vertical registers for the CRAF/Cassini CCD showed less of an improvement since the main vertical channel width is only 9-microns accounting for channel stop width.

It is interesting to note that notch technology is also used to improve CTE performance for large CCD arrays. For example, large 2048 x 2048 and 4096 x 4096 Loral pixel devices have included notch channels for improved CTE response. CTE's as high as 0.9999995 have been measured for these devices, the highest CTE ever achieved by a CCD.

CTE performance can be predicted for a given radiation environment and shielding arrangement by using *CCD radiation transfer curves*. One such curve which has been extremely beneficial in radiation analysis and prediction is the *proton transfer curve* (the proton is the dominant particle found in space). The curve plots the average number of displacements for an interacting proton as a function of it's energy (10 keV to 1 GeV). The curve, for example, shows that a 250 keV proton is the most damaging to a frontside illuminated CCD where on the average 13 silicon displacements per proton are induced in the sensor's signal channel 1.5-microns in extent. A 100 MeV proton is 1000 times less damaging since its *non-ionizing energy loss* (i.e., energy that goes into the production of silicon vacancies per unit length) is considerably less than a 250 keV proton. The proton transfer curve is accompanied by another curve that plots the number of silicon displacements required to produce an *active trap* as a function of proton energy (referred to as the *radiation trap inefficiency (RTI) curve*). The RTI curve shows that it takes roughly 400 silicon displacements before an active electron trap is made and becomes influential on CTE (these data are based on the CRAF/Cassini CCD, however, other CCD types exhibit similar properties). The proton transfer curve is used extensively in radiation studies to assess CCD performance assuming different shield thicknesses and materials applied in various radiation environments.

Other radiation transfer curves for the CCD have been generated. For example, *neutron and gamma-ray transfer curves* have been used by Galileo and CRAF/Cassini because of radiation events made by on-board Radioactive Thermal Generators (RTG's) used to generate electrical power on the spacecraft. RTG's generate 2 MeV neutrons and gamma-rays, particles and photons that are also very damaging to the CCD.

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CTE Test Tools

Several CTE test tools have been invented to measure CTE performance for the CCD. The majority of these test methods compare the quantity of charge contained in a target pixel to the quantity of deferred charge following that pixel after many transfers have been executed. These techniques are referred to as *relative CTE test methods* because absolute charge levels are not measured. Experience has shown that relative CTE measurements often lead to erroneous CTE figures and have mislead the user in how well the sensor is actually performing. For example, if CTE for bulk-state limited CCD is measured at an operating temperature where the bulk emission time constants are longer than the pixel transfer period then deferred charge will be spread over many trailing pixels. The deferred charge tail for the sensor may be hidden in the sensor's read noise floor and as far as the user knows perfect CTE is exhibited. CTE behavior for the designed induced trap associated with the Space Telescope CCD is a good example of this phenomenon. Numerous TI 3PCCDs were tested that achieved apparently good CTE since the sensors did not exhibit deferred charge tails. In fact the WF/PC I CCDs flown on Space Telescope were tested and screened using this criteria, that is, the shorter the deferred tail the better the CCD. This rule is not followed today. Testing of flight spare units several years later revealed that the transfer gate design trap was abnormally deep for CCDs without tails so that signal charge escaped very slowly and remained hidden in the read noise floor. In fact some of these CCDs could completely swallow a low-light level star image (< 100 e-) without any indication that it was really there.

The only guaranteed method to measure *absolute CTE* and avoid CTE surprises like those discussed above relies on x-ray stimulation of the CCD where a known amount of charge is generated in a pixel. For example, an Fe-55 x-ray source produces a 5.9 keV photon and when interacting with the CCD generates 1620 e- in a volume much smaller than a pixel (the perfect impulse stimulus). Absolute CTE is measured with an Fe-55 source by simply stimulating the CCD uniformly with x-rays and reading the charge contained in each pixel. Ideally, if a pixel initially contains 1620 e- then it should contain the same amount of charge after being transferred to the output amplifier. However, if charge is lost in the transfer process a CTE problem exists. The ratio of charge measured in a pixel to 1620 e- divided by the number of pixel transfers is defined as the *charge transfer inefficiency* (*CTI*) per pixel transfer. CTE is simply (1 - CTI). This definition is used to measure *global CTE* characteristics where during each pixel transfer an given amount of charge is displaced from the target pixel. This quantity may be very small in each

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pixel transfer but becomes appreciable when many transfers are executed. For example, a CTE of 0.999999 translates to only 0.001 e- per transfer assuming an initial charge level of 1620 e. If 4096 transfers are executed a net loss of 41 electrons will be measured, readily detected from *x-ray histogram plots*.

X-ray stimulation is also important in identifying process and design induced traps discussed above. As mentioned above, relative CTE measurement techniques may not find isolated traps because the trap may not show a deferred charge tail. With x-rays each column of the array can be stimulated and characterized for traps to assure that the CCD is trap free.

Other CTE tests have been invented in measuring CTE for ultra-small charge packets. For example, the *extended pixel edge response (EPER)* allows one to estimate the CTE in transferring a single electron in the CCD. For example, the CTE for a single electron for a bulk state limited CRAF/Cassini CCD has been measured at 0.995.

In general CTE degrades for smaller charge packets. Charge transfer loss in CCDs is best described as a combination of a *proportional* and a *fixed* loss of charge depending on the CTE problem experienced (23). Fixed loss is independent of the charge packet size. Here a fixed amount of charge is lost, characteristic of the localized trap. Proportional CTE loss (also referred to as fractional loss) is proportional to the size of the charge packet transferred. That is, if 500 e- are deferred for a 10,000 e- charge packet, then 5000 e- will be deferred for a 100,000 e- charge packet. Proportional loss best describes CTE loss incurred by bulk traps when relatively large charge packets are transferred. This results in a constant CTE with charge level for the device. A combination of fixed and proportional loss is involved for small charge packets where CTE decreases with signal level.

While a very small trap may not be detected by x-ray characterization, it can be clearly located by the technique of *pocket pumping*. This method amplifies the effects of a trap and can map the exact position, size and even the location of the defect within the pixel for traps 1 e- or less in size. Pocket pumping is performed by first exposing the CCD to a low-level flat field of approximately 100 e- depending on the size of the trap to be detected. After the exposure the CCD is clocked backwards a specified number of lines and then run forward the same number of lines to the original image position (referred to as a line sector). This clocking scheme is repeated many cycles before the CCD is finally read out in the normal fashion. The

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backwards and forward clocking causes the signal charge to build up or be pumped in a trapping site. The rate of charge buildup is directly proportional to the trap size. For example, a 1 e- trap will produce a 200 e- signal if "pumped" 200 times. It should be noted that pocket pumping can only be performed on *bi-directional* CCDs where charge can be transferred upwards or downwards in the array (virtual phase and two phase CCDs are uni-directional).

Pocket pumping tests are performed on a regular basis to verify that CCD lot runs are fabricated on silicon wafers with minimum bulk trap counts. In specifying todays CCD silicon a *silicon quality factor (SQF)* is often used to insure that well-behaved CTE performance is achieved. For example, SQFs of less than 0.002 traps/pixel are specified for the CRAF/Cassini CCD at an operating temperature of -60 C using the pocket pumping technique. SFQs of this level guarantee that CTEs of five nines or better will be achieved (assuming that the sensor is bulk state limited and is not plagued with other CTE difficulties such as processed induced traps).

8. READ NOISE

Random noise places a lower limit on the smallest charge packets that can be detected and measured by the CCD. Many noise sources external and internal (24, 25) to the CCD can contribute to this limit). These sources can be grouped into three major categories. The first group are referred to as intrinsic noise sources inherent to the CCD and processing electronics. Some good examples of intrinsic noise are thermal, 1/f, photon and dark current shot noise, spurious charge, and ADC quantizing noise. The second noise group to consider are man made noise sources or interference noise. Examples of these types of noise are boundless and include radio and TV broadcast interference, ignition, power line (e.g., 60 cycle), motor, switching systems (e.g., micro-processors), etc. The third category are noise sources related to natural disturbances, such as cosmic rays, lightning, etc.

For optimum performance, it is desirable that the noise sources listed above be reduced to a minimum. Eliminating noise from a CCD camera system is like "peeling an onion" since the CCD engineer begins with the highest noise source present and diligently works towards the CCD on-chip amplifier read noise floor. Quite often a half-dozen or more noise sources may be encountered in the noise reduction process.

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On-chip Amplifier Noise

The read noise of the CCD is ultimately limited by the noise generated by the on-chip output amplifier. Today several manufacturers are fabricating CCD amplifiers that exhibit noise levels of 3 e- rms and lower by clocking the CCD slow-scan (<50 kpixels/sec). Reducing the noise to this level is an amazing accomplishment considering that noise levels observed in the early days of CCD development were over an order of magnitude greater than this. At that time it was believed that read noise improvements of any significance were unlikely based on theoretical grounds. However, new process and design advancements for the CCD were not anticipated which permitted lower noise floors to be achieved.

Amplifier read noise is dependent on three factors: the thermal white noise and flicker (1/f) noise associated with the on-chip *metal insulator silicon field effect transistor* (*MISFET*) amplifier, and the sensitivity of the sense node. The sense node is a n+ diffusion located at the end of the horizontal register and represents the final collecting well for all charge packets. The capacitance associated with the diode converts signal charge into a working voltage (i.e., Volts = charge/capacitance). The sense node sensitivity ranges from 1 to 4 micro-volts per electron for most scientific CCDs fabricated today. The sense node is directly connected to the input of the MISFET amplifier. In that the sense node precedes the amplifier, the read noise (in rms e-) is inversely proportional to the node sensitivity. White and 1/f noise are primarily dependent on the size of the on-chip amplifier and, in general, can be reduced by making the amplifier physically larger. On the other hand, the input capacitance of the amplifier increases as the amplifier geometry grows which in turn lowers node sensitivity increasing the net read noise.

The challenge at CCD manufacturers was to find an optimum amplifier geometry that yielded the lowest noise (rms e-) by minimizing 1/f and white noise generation and at the same time maintain high node sensitivity. Although MISFET design equations were used initially by several CCD groups in calculating the optimum amplifier size, the most productive work came from experiment. In these experiments several on-chip amplifier structures with differing geometries were fabricated and tested using the TI 3PCCD as a baseline for comparison (this CCD achieved a noise figure of 13 e- rms). During this optimization process it was discovered that if the on-chip amplifier was made smaller that the contributions of white and 1/f noise increased at a slower rate than the node sensitivity increased resulting in lower read noise. This trend continued until the read noise began to increase indicating the amplifier's geometry was too

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small. The optimum geometry found was roughly a 6 (channel length) x 65 (channel width) amplifier that yielded approximately 4 to 5 e- rms read noise. For comparison the geometry of the TI 3PCCD on-chip amplifier is larger: 11 (L) x 120 (W) -microns. Curiously Tektronix, Lincoln Labs, and Loral have all run these studies and have independently settled on basically this same amplifier size for lowest noise.

Although these design improvements in noise reduction were worthwhile, significant advancements were also made in how the amplifier was processed. Two refinements were fruitful. First, the *1/f noise knee* of the amplifier was reduced to lower frequencies. For example, current scientific CCDs exhibit a 1/f noise knee about 10 kHz. For comparison the Space Telescope TI 3PCCD noise knee is approximately 100 kHz. The reason behind the improvement is not totally clear, however, it is believed that processing improvements have been directly responsible specifically the passivation of the surface states at the Si-SiO_2 interface is one possibility. It is generally accepted that 1/f noise is generated at the surface (via channel current interaction with surface states) since very high 1/f noise knees were observed for surface channel MISFET amplifiers made by RCA originally (these amplifiers exhibited 1/f noise knees of several MHz). For buried channel devices 1/f noise is considerably lower. There is also the possibility that some 1/f noise is generated within the *pinch-off region* or in the drain diffusion of the MISFET itself, weak avalanche regions where high fields are found.

The second process factor that improved amplifier noise uses a processing technique referred to as *lightly doped drain* (*LDD*), a doping technology used by the semiconductor industry for many years. LDD reduces parasitic gate capacitance associated with the drain and source regions of the MISFET amplifier. LDD technology increases the node sensitivity (about a factor of two for the 6 x 65-micron amplifier described above) without increasing the noise characteristics of the amplifier (i.e., 1/f and white). LDD amplifiers in conjunction with optimum geometry have pushed CCD read noise to less than 2 e-. The majority of CCD groups that employ LDD technology include GEC, Lincoln Laboratory, Tektronix, and Loral.

In theory 1/f noise should not be present in buried channel CCD amplifiers since the channel current is confined to the bulk (this assumes that 1/f noise is surface state related). Since 1/f noise is seen the main question asked today is where in fact does 1/f noise come from. One possibility is the noise is generated at the source and drain contacts, locations where the channel current interacts with the surface. Wherever the source,

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this area of research will remain active since 1/f noise limits the ultimate read noise that can be achieved by the CCD. If 1/f noise was not present, then white noise associated with the amplifier could be reduced without limit by simply reducing the electrical bandwidth of the CCD signal processor in conjunction with increasing the sampling period for each pixel read (read noise would then decrease by the square-root of the sample period). However, when 1/f noise is present the read noise becomes limited when the sample time becomes appreciable to the period of the 1/f noise frequency knee. At this point read noise becomes invariant with sample time and bandwidth adjustment. The read noise will actually increase with sample time if the slope of 1/f noise is greater than unity (e.g., $(1/f)^{1.5}$, a characteristic of a CCD amplifier that is biased to high and is breaking down).

Noise Measurements

Lincoln Laboratory appears to hold the record for the lowest noise achieved by the CCD; 1.5 e- rms, close to the 1 e- level that CCD groups have been trying to achieve. These noise measurements were performed by the MIT CCD group. JPL has measured the same CCD at 1.7 e- rms in close agreement to MIT. Noise measurements this low are touchy to perform and depend on several factors including the noise performance of the CCD signal processor (*signal chain*) used in making the measurement. Signal chains used for low noise measurement must exhibit equivalent noise levels much less than 1 e- rms. Also precise calibration of the signal chain is necessary in converting output digital numbers (*DN*) generated by the camera's analog digital converter (ADC) to rms electrons (i.e., e-/DN = *camera gain conversion constant*). This calibration procedure is performed by using the *photon transfer technique*. Photon transfer has also demonstrated to be the most valuable test tool in calibrating, characterizing, and optimizing scientific CCDs. In addition, photon transfer is usually the first test performed in characterizing the over-all performance and health of a new CCD camera system and is routinely used as a diagnostic test tool in locating camera problem areas, such as noise (references are provided at the end of this paper that discuss the photon transfer method and noise reduction techniques).

Skipper CCDs

Although it appears that future developments might eventually reduce the read noise of the CCD to 1 electron by optimizing on-chip amplifier parameters (i.e., white - 1/f noise and node sensitivity), it is unlikely that the read noise floor will be reduced significantly below this level using conventional

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detection schemes. A new technique now being incorporated on CCD structures is based on a *nondestructive readout amplifier*, a read out approach which has driven the read noise floor significantly below the 1 e- level. The idea is nearly two decades old, it is only now where nondestructive readout schemes become advantageous since on-chip amplifier noise characteristics have been pushed to their limit. Referred to as the *Skipper CCD*, the sensor allows one to measure a charge packet several times by shifting the charge packet back and forth between two gate electrodes, one of which is a *floating gate* (26) connected to a conventional MISFET amplifier and the other gate which acts as a *storage gate* for charge to shift to. Charge for one pixel is transferred back and forth between these two gates. Each time charge is dumped on the floating gate a video sample is taken. Averaging many samples for the same pixel allows one to achieve a read noise floor to any level desired depending on the number of samples acquired. For example, if 100 samples are averaged together the read noise is effectively reduced by a factor of 10. Noise floors of less than 0.5 e- rms have already been demonstrated using the approach which have allowed 2 to 3 e- charge packets to be detected. New improved Skipper CCDs will hopefully be able to achieve noise levels of a tenth of electron so that individual photoelectrons can be detected. This work has been prompted by NASA for the CUBIC mission mentioned in Chapter 1.

The Skipper CCD has circumvented the 1/f problem mentioned above since a shorter sample period can be used for each pixel, short enough to remain out of the 1/f noise regime. However, the penalty paid is each pixel must be sampled multiple times (the noise is cut by the square-root of the time spent on each pixel - similar to if the CCD was white noise limited). It should be noted that conventional *floating diffusion* (27, 28) amplifiers only allow one sample to be taken because once charge has been transferred to the sense node charge cannot be pulled out and resampled again (i.e. *destructive amplifier*).

In practice multiple-sampling of pixels is performed on a pre-selected region on the array that requires further interrogation and signal-to-noise (S/N) improvement. This process begins by taking a full frame of data using single pixel samples. The data from the frame is reduced and a region of interest is selected. Then a second frame of data is taken and the region is multiple sampled improving the S/N. The remaining pixels are "skipped" and discarded. In this manner the frame readout time can be reduced.

It should be also mentioned that Skipper CCDs will not significantly improve the S/N for low-level "extended" images. This is because the shot noise of the signal becomes dominant.

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For example, a 1 e- signal will generate 1 e- worth of shot noise resulting in a S/N = 1 producing a "grainy" image. Reducing the noise floor further by means of multiple sampling will only slightly improve the S/N. For instance, the S/N of a 1 e- signal in conjunction with a 2 e- amplifier will yield a net S/N = 0.45 compared to S/N = 0.98 when 100 samples are taken, not a significant improvement in terms of improving image quality.

The Skipper CCD is advantageous in terms of S/N when measuring point source images or measuring x-ray events. For CCD-RIS applications lower read noise translates into improved energy resolution. As mentioned above new Skipper CCDs have been designed and are currently under test to detect a single photoelectron the ultimate energy resolution for the CCD (the CCD would also compete with photomultiplier sensors).

Dark Current Noise

As introduced above, there are several types of intrinsic noise sources. One important source generated internal to the CCD is dark current. Dark current is due to thermally generated electrons within the device and represents an inherent limitation on read noise performance due to the *dark shot noise* that is produced. Thermally generated charge is governed by Poisson statistics (as is *photon shot noise*).

For CCD imagers there are three main sources of dark current within the device. These are (1) thermal generation and diffusion in the neutral bulk, (2) thermal generation in the depletion region and (3) thermal generation due to surface states at the Si-SiO_2 interface. Of these sources, the contribution from surface states is the dominant contributor for CCDs fabricated in the past. *Surface dark current* is between two to three orders of magnitude greater than dark current generated by the bulk of the CCD (i.e., *bulk dark current*).

Dark current generation at the Si-SiO_2 interface depends on two factors, namely the density of interface states and the density of free carriers (holes or electrons) that populate the interface (29). Electrons that thermally "hop" from the valence band to an interface state and then to the conduction band will produce an e-h pair that will be collected in the potential well. The presence of free carriers will fill the interface states inhibiting the *hopping conduction* mechanism and, in turn, substantially reduce dark current generation to the bulk rate level. *Noninverted* CCDs (i.e. where the clock bias is such that the surface potential at the Si-SiO_2 is greater than substrate potential) deplete the interface of free carriers, maximizing surface dark current generation. Under depleted conditions, dark

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current generation is solely a function of the density of interface states at the Si-SiO_2 interface. When the CCD is inverted, as discussed in Chapter 2, holes from the channel-stop regions migrate and populate the Si-SiO_2 interface eliminating hopping conduction and surface dark current generation. Under these conditions the device is said to be *bulk dark current limited*.

Multi-phase CCDs can be biased into a mode referred to as *partially inverted*. For a three-phase CCD partial inversion is accomplished by biasing a collecting phase high (say phase 1 = 3 V) and biasing two barrier phases into inversion (say phases 2 and 3 = -8 V). Inverting two barrier phases reduces dark current generation by 2/3. The partially inverted mode also leads to optimum full well performance for the CCD as discussed below.

Multi pinned-phase (MPP) CCDs can operate *totally inverted* to achieve ultra-low dark current generation rates. MPP-CCDs are processed slightly differently than conventional devices for the following reason. If all three phases of a 3PCCD are inverted (say all phases at -8 V) there is no collecting well since the potential wells beneath each phase are equivalent and exhibit no well capacity. Hence, in this bias condition blooming would occur as soon as the CCD was exposed to light. To obtain well capacity while totally inverted the potential of one or more phases must be offset from the others. For a three-phase MPP-CCD this can be accomplished by doping the silicon beneath phase 3 with boron. The boron in effect neutralizes the phosphorus dopant in the channel reducing the potential in the region. When biasing all phases into inversion charge will now collect under phases 1 & 2 and be confined by phase 3 which acts as the barrier phase. Phase 3 will attain inversion before phases 1 & 2 as the clocks are driven negatively. For Loral and Tektronix CCDs total inversion occurs at -6.5 V for phase 3 and approximately -8 V for phases 1 & 2. The channel potential is offset by approximately 2.5 V between phase 3 and phases 1 & 2 established by the amount of boron implanted. It should also be noted that a three-phase MPP-CCD can also be fabricated by implanting phase 3 with additional phosphorus forcing charge to collect under this phase (phases 1 & 2 would then act as the barriers). Loral and Tektronix MPP-CCDs are based on a MPP boron implant. Four-phase MPP-CCDs have also been fabricated in a similar fashion at EG&G Reticon.

MPP-CCDs can also operate partially inverted as described above. However, for proper operation the positive clock level of phase 3 should be offset by the *MPP built-in potential*. For Loral and Tektronix CCDs, the positive rail of phase 3 should be clocked 2.5 V higher than phases 1 & 2 if partial inverted clocking is

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utilized.

It should be noted that the full well capacity of a MPP-CCD is determined by the MPP built-in potential. Operating totally inverted will yield well capacities that are two to three times lower compared to when the device is partially inverted depending on pixel size. Future development work is required to achieve greater well capacities for the MPP-CCD by increasing the MPP implant dose.

Dark current rates achieved by MPP-CCDs is significantly lower than the dark rates achieved by the TI 3PCCD. The dark current generation rates for the Space Telescope CCD ranged as high as 15 nA/cm^2 at room temperature when noninverted (*inverted clocking* was not invented at this time and therefore surface dark current generation was maximized). These sensors required cooling to -40 C before images could be taken - dark current rates greater than three-orders magnitude compared to MPP-CCDs. Such performance has offered several practical benefits to WF/PC II. For example, the camera can now be aligned and focused at room temperature without requiring cooling. In addition, cooling requirements for WF/PC II and future space missions are significantly relaxed when MPP operation is used. For example, WF/PC II is planning to cool to -65 C compared to -100 C to achieve the same specified dark current generation rate of 0.01 e- sec/pixel. Contamination of the CCD in flight is also less concerning at warmer temperatures. Because the WF/PC CCD is the coldest element of the camera system it attracts water and hydrocarbons that out-gas from the instrument once in orbit. Contamination on the CCD window due to this problem plays havoc with UV sensitivity (WF/PC I exhibits poor UV sensitivity because of this adversity). By operating the CCD at warmer temperatures condensation on the window is reduced considerably.

MPP-CCDs are being manufactured by most CCD manufacturers. Some rather amazing images have been generated by these devices. For example, the Loral 1024 x 1024, 15-micron pixel, MPP-CCD can integrate for 8 minutes at room temperature before reaching full well and saturating with dark charge. MPP-CCDs have been substituted for photographic film in 35-mm cameras. Because MPP-CCDs can be slow-scanned the control logic and processing electronics can be low-power and compact (such a camera has been interfaced to a 486-PC, a powerful but relatively inexpensive little scientific CCD camera system). MPP-CCD cameras have been utilized behind amateur astronomical telescopes without cooling and vacuum heads. Room temperature operation opens up a number of new possibilities for the scientific CCD in the future.

It should be mentioned that bulk dark current generation is

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highly dependent on the quality of silicon used in fabricating the CCD. Experience has shown that low bulk dark generation does not come routinely. For example, MPP-CCD lots fabricated at Loral have shown a wide variation in bulk dark current generation rates from wafers fabricated from the same silicon foundry. CTE and bulk dark current generation are correlated since both parameters are related to bulk states exhibited in the silicon. As discussed before, the silicon wafers should be screened before a full production run of CCDs is made to avoid surprises.

Spurious Charge Noise

Total inversion achieved by MPP technology can also be realized by VPCCDs, OPPCCDs and two-phase CCDs. When a CCD phase is driven into inversion, holes from the channel-stops migrate and collect beneath the gate pinning the surface to substrate potential. Some of these holes become trapped at the Si-SiO_2 interface. When the clock is switched to the noninverted state to transfer charge the trapped holes are accelerated out of the Si-SiO_2 interface. Some holes are released with sufficient energy to create electron-hole pairs by means of a mechanism called *impact ionization*. These spurious electrons are then collected in the nearest potential well. This very important source of charge generation in CCDs is referred to as spurious charge.

There are a number of characteristics associated with spurious charge that are important to know in regulating the amount of charge generated. First, spurious charge is only generated on the leading edge of the drive clock, that is, when the phase assumes the noninverted state and holes are forced back to the channel stop regions. The falling edge has no influence on spurious charge generation in CCDs. Second, spurious charge increases exponentially with clock rise time and voltage swing. Sending holes back to the channel-stops with a fast moving, high amplitude clock increases impact ionization. Third, spurious charge increases with clock width or the amount of time the clock remains in the noninverted state. This is because more time is given for holes to escape from the interface resulting in more spurious charge. If the clock width is short holes will remain in the interface states without causing impact ionization. Forth, spurious charge increases as the operating temperature of the CCD is lowered. Here theory indicates that impact ionization is more efficient at colder temperatures. Fifth, spurious charge generation occurs each time signal is transferred between phases, and therefore the amount of spurious charge that is collected increases linearly on the number of transfers that take place. Sixth, and the most critical to read noise performance, is the noise this phenomenon produces can be characterized as shot

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noise, i.e., the noise increases by the square-root of the spurious charge generated.

Spurious charge generation adds up quickly when generated in large arrays and therefore must be controlled if on-chip amplifier noise is to dominate. For example, assume on the average only 0.1 e- of spurious charge is generated during each pixel transfer (i.e., for 10 pixel transfers a single electron is produced on the average). For 1024 transfers this would generate 107 e-/pixel translating to a read noise floor of 10 e- rms limiting the noise floor to this level.

There are three methods used to reduce the shot noise produced by spurious charge to negligible levels. One method is to tailor the rise time of the drive clocks and allow the holes to go back to the channel stop regions slowly (this is usually accomplished by adding a simple R-C network at the output of each CCD clock driver). The second, clock swings should be limited to the smallest range possible without jeopardizing CTE performance. In this manner the electric fields in sending holes back to the channel-stops are weaker generating less spurious charge. Third, the trapped holes can also be ameliorated by use of a *tri-level* clocking scheme. This technique uses a intermediate clocking voltage, which lies between the high and low clock rails required for complete charge transfer and at voltage which is just above the inverted state. The rising edge of the transition from the lowest voltage to the intermediate voltage should occur with a reasonably long time constant (several micro-sec), which allows the trapped holes to be released slowly from the oxide minimizing spurious charge generation (the Galileo CCD required this clocking technique to keep spurious charge to acceptable levels).

With these solutions in mind spurious charge generation can usually be reduced to negligible levels (i.e. *spurious shot noise* less than the read noise of the on-chip amplifier). The vertical registers of the CCD are normally inverted to achieve low dark current characteristics. Spurious charge generation for these registers is small because the clock waveforms to the array are inherently slow due to the high capacitive load associated with the imaging pixels. The horizontal registers are clocked at faster rate and if operated inverted would generate significant amounts of spurious charge severely limiting the read noise floor. Therefore, the horizontals of a CCD are always operated noninverted since dark charge in these registers is not important. For this reason the horizontal registers of a MPP-CCD never receives the MPP implant since they are never inverted.

For VPCCDs the situation is quite different. Unfortunately the

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horizontal register of a VPCCD must be switched in and out of inversion to transfer charge resulting in spurious charge generation and limiting read noise performance. For example, the read noise of the 800 x 800 pixel Galileo VPCCD is dictated by spurious charge at 30 e- rms using tri-level clocking (i.e., 900 e- of spurious charge is generated in 800 pixel transfers, slightly more than 1 e- per transfer). Galileo's on-chip amplifier, however, can achieve a 10 e- rms level a level that couldn't be realized by Galileo because of spurious charge.

9. FRONTSIDE PINNING

Inverted technology or frontside pinning offers many other benefits to the user other than low dark current generation discussed in Chapter 8. Additional CCD parameters influenced by frontside pinning include *surface residual image*, *pixel nonuniformity,* full well capacity, and blooming to name a few. Also pinning increases the CCDs tolerance to high energy radiation and allows the CCD to be rapidly erased. We will address some of these benefits in this chapter.

Residual Image

Residual image occurs when the CCD is over-exposed to light or when the buried channel becomes undepleted (i.e., when CCD bias to the n-channel is removed). Under either of these conditions, electrons will get trapped at the frontside Si-SiO_2 interface. The trapped charge will be released slowly and will be seen as a residual image in subsequent long dark integration periods. When the CCD is operated at cold temperatures the trapped charge may take several hours or even days to escape (the emission time constants of interface traps increase exponentially with decreasing temperature). In fact residual images have been seen at Palomar Observatory a week after a TI 3PCCD was over-exposed to a star-field and left cooled at -140 C. With inverted clocking applied (via partial inversion or MPP) holes recombine with the trapped electrons eliminating all surface residual image effects. Residual image is erased during the first line transfer when all phases of the CCD have gone through the inverted condition.

Full Well Capacity

Full well capacity for multi-phase CCDs has improved significantly since the sensor has been inverted and pinned. As mentioned in Chapter 2, the well capacity of a pixel is defined when either blooming or surface channel operation occurs depending on the positive bias to the collecting phase. For example, if the

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collecting phase is biased so its surface potential is greater than the channel potential of the barrier phase then charge will interact with the surface before blooming occurs. Surface full well shrinks when the gate potential of the collecting phase is further elevated because the channel potential shifts towards the surface. In the limit surface full well is reduced to zero at some high clock bias (approximately 20 V for Loral CCDs) where the surface and channel potentials of the collecting phase become equivalent. At this point the CCD runs totally surface channel.

When the surface potential of the collecting phase is adjusted below the channel potential of the barrier phase then blooming will result (i.e., charge will spill into neighboring pixels before charge reaches the surface). Lowering the clock drive to the collecting phase further reduces this potential difference and well capacity.

From the discussion above optimum full well for a multi-phase CCD is achieved when blooming and surface full well occur simultaneously. That is, when the surface potential of the collecting phase equals the potential maximum of the barrier phase. For Loral and Tektronix CCDs this condition occurs when the barrier phase is biased into inversion (typically -8 V) and the collecting phases are biased positively (typically at 3 to 4 V). It should be noted that the surface potential of the collecting phase is initially greater than the channel potential of the barrier phase when the collecting well is empty. As the collecting well fills the surface potential decreases approaching the channel potential of the barrier phase. Optimum full well occurs when the two potentials become equivalent. Several test methods have been invented to find the optimum full well point. One such method will be described below (refer to anti-blooming).

Biasing the CCD in the manner described above will significantly increase well capacity for the sensor over bias schemes used in the past. For example, the well capacity for the TI 3PCCD can be increased by a factor of three over what is currently flown on Space Telescope by simply clocking the CCD into inversion (currently the vertical registers of WF/PC I CCD are clocked from ground potential to 7 V and achieve a well capacity of about 30,000 e-). The well capacity for the new Loral WF/PC II CCDs has improved enormously due in part to how the CCD is biased in obtaining optimum full well capacity (an improved pixel design and process are two other reasons). Full well achieved for these sensors is over 300,000 e- a factor of ten times higher than currently achieved based on the same pixel size (15-microns). This capacity in conjunction with an improved noise floor (3 e- rms compared to 13 e- rms) yields a dynamic range of 100,000 (compared to the present dynamic range of 2308).

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New CCD design and process developments are likely in the near future to drive the well capacity even higher for the sensor. It is known that increasing the phosphorus doping of the signal channel increases full well capacity. However, there is a limit to how much doping can be employed because the electric fields generated internal to the device also increase. If the electric fields are too strong breakdown will result leading to excessive dark current generation. The fields are strongest in the region where the channel stops and signal channel meet. It is at this interface where dark spike generation is likely. Measurements show that silicon lattice defects in conjunction with high fields lead to dark spikes. Defects promote hopping conduction whereas the fields assist in the generation process (referred to as *field assisted* dark current generation). Virtual phase CCDs exhibit high dark current spikes since these sensors are doped near breakdown to achieve high well capacity. Characterization tests show that the dark spikes are generated entirely within the virtual region of a pixel, a regime where high dopants and fields are found.

A new CCD technology, referred to as the *Super Notch,* is currently under development to increase well capacity via doping and at the same time maintain low dark spike generation. The super notch is a derivative of the Notch CCD discussed in Chapter 7. In its design the width of the notch is enlarged just short of the channel stop regions leaving lightly doped material between it and the channel stops. It is hoped that the super notch can be heavily doped to achieve high full well without an increase in dark spike generation. The super notch may also be beneficial in curing those dark spikes induced by high energy radiation events.

Anti-blooming

As discussed in Chapter 2, blooming will occur when the channel potential of the collecting phase is reduced below that of the barrier phase. This condition leads to charge spreading up and down the column (e.g., a common problem when bright star fields are imaged). A multi-phase CCD can be clocked during integration to eliminate image blooming using the following clocking technique. During integration the barrier phase (phase 3) remains pinned and inverted at all times. Phases 1 & 2, however, are slowly switched between the inverted state and slightly above the optimum full well level (typically -8 V to 5 V for Loral, Lincoln Laboratory, and Tektronix CCDs) running slightly surface channel when full well is exceeded. Signal charge therefore transfers between phases 1 & 2 during integration being confined within a pixel by phase 3. At any instant of time charge builds up within one of the two phases being clocked (for purposes of discussion say charge collects in phase 1 with phase 2 inverted)

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until a level of charge is reached when surface full well is exceeded. At this point charge enters the gate oxide beneath phase 1 with some of it becoming trapped at the $Si\text{-}SiO_2$ interface. Phases 1 & 2 are then switched, inverting phase 1 (-8 V) and biasing phase 2 high (5 V) to collect charge. Signal charge in phase 1 now moves to phase 2 except for trapped electrons still under phase 1. As phase 1 inverts holes populate the interface recombining with the trapped electrons. At the same time signal charge is builds up under phase 2, starting at surface full well. Charge beneath this phase now enters the oxide and becomes trapped. Phases 1 & 2 are then switched again forcing phase 2 to invert obliterating trapped charge there by holes. This clocking sequence continues throughout the entire integration period. As long as the clock frequency of phases 1 & 2 keep pace with charge generation rate blooming is inhibited for the CCD since the charge level in phases 1 and 2 is kept near the surface full well state.

The required switching rate of phases 1 & 2 depends on how fast charge is generated in a pixel. Experiment has shown that every few milliseconds is sufficient for most slow-scan CCD applications. For example, Loral CCDs require a 50 Hz rate to control blooming for charge generation rates of 2,000,000 electrons/sec. This figure assumes a positive rail of 1.5 V above the optimum full well level. Greater efficiencies can be obtained when the positive rail of the collecting phase is set higher since more signal charge is allowed to enter the $Si\text{-}SiO_2$ interface. However, as mentioned above, when the collecting phase is biased higher the well capacity is reduced.

The anti-blooming clocking technique becomes limited when the integration periods are short (e.g., commercial 1/30 sec rates) or when the CCD is strobed. For these situations it becomes difficult to pump charge into the oxide and invert the device fast enough to keep pace with the charge generation rate (it also becomes more difficult to control spurious charge generation since the clock edges must slew at a faster rate). Therefore, these applications might require built-in *anti-blooming drains* employed in each pixel. However, these custom CCD structures take up valuable real estate on the chip reducing the *fill factor* of the pixel (i.e., that part of the pixel that is photosensitive) translating into lower QE. The anti-blooming clocking technique described above maintains a fill factor of 100 %.

The anti-blooming clocking technique was successfully employed in the ESC camera mentioned in Chapter 1. For this CCD application anti-blooming was necessary since bright spots from reflected sun light were expected in the space shuttle images taken. Exposure

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times employed were relatively fast (1/100 sec) and the anti-blooming clocking technique only provided blooming protection up to approximately 200 times full well capacity. The anti-blooming technique will also be used in all ISS CRAF/Cassini CCD cameras including the VIMS CCD camera. Since the integration periods employed by these cameras are relatively long, anti-blooming will achieve a greater dynamic range than the ESC camera. CRAF/Cassini, for example, expects to hold back blooming to over 1000 times full well.

The anti-blooming clocking technique effectively increases the dynamic range for the CCD. For example, deep exposures have been taken of very dim objects next to bright objects (e.g., a dim moon next to its parent planet) that exceed full well by three orders of magnitude. Experiment has shown that light scattering and ghost images generated internally to the camera limit how deep an exposure can be made.

The anti-blooming clocking technique is a useful test tool in optimizing full well capacity of the CCD. To perform this measurement the CCD is first over-exposed to a bright source of light allowing all pixels to saturate. The light is then turned off (or shutter closed) and the anti-blooming clocking technique applied for a second or two. During this time charge above surface full well is consumed by the holes forcing the charge level within a pixel back to the onset of surface full well. The frame of data is then read out and the charge for each pixel measured. The resultant image produced is a *pixel full well map*. Optimum full well is achieved by performing the same experiment several times while adjusting the positive clock rail until an optimum point is found.

High Speed Erasure

On occasion it is necessary to erase the CCD as quickly as possible, an important mode of operation when clearing large CCD arrays of charge. Other high speed clocking applications require the CCD to be read out quickly to a region of interest discarding all pixels up to and beyond the subpixel array interrogated. For example, star tracking CCDs function this way where a low-level star image might be measured many times a second for navigation purposes.

High speed erasure or clocking is performed by clocking the vertical registers as fast as possible dumping charge into the horizontal register. It is important that when the CCD is clocked in this manner that horizontal charge back-up problems into the array does not occur. This characteristic typically results when the horizontal charge transfer rate can't keep up

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with the charge being transferred from the vertical registers. Charge back-up problems limits how fast charge can be removed from the array in a controlled manner. For example, if charge back up occurs it may take several frame erasures to erase the CCD of unwanted charge. Virtual phase CCDs are difficult to erase because of charge back-up problems. For example, a saturated Galileo VPCCD requires approximately 10 frames of readout before all charge is erased from the array (the Galileo erase time is set by the horizontal clock rate which is a couple Mpixels/sec). As we will discuss below, todays multi-phase CCDs can be clocked such that all charge is removed in a single frame readout at any vertical clock rate employed.

High speed erasure can be performed efficiently using the following inverted clock scheme. To erase the CCD the vertical registers are clocked from the inverted state to a positive clock level (e.g., -8 V to +3 V). The vertical clock rate can be at any rate desired in moving charge down to the horizontal register. The clocks of the horizontal register are clocked noninverted (say -4 to +5 V). In that the potential of the horizontal barrier phases is less than the barriers of the vertical phases charge will flow into the horizontal register unimpeded even if the horizontal register is saturated. To remove charge from the horizontal register the reset MISFET is clocked even less negatively (say 0 to 10 V). Charge from the horizontal register will then spill through the reset gate and out to the reference supply off chip. In effect by biasing the CCD in this way the horizontal and reset gate act as drains for vertical charge that is transferred. The horizontal register need not be clocked fast to keep up with the vertical charge rate, in fact, the clocks can be inhibited to either the high (+5 V) or low (-4 V) state if desired. As long as the negative horizontal rail is less than the vertical rail (-8 V) then charge will naturally diffuse into the horizontal register whether it is full or not. Similarly the reset clock does not need to be clocked as long as its low level (0 V) is less than the low level of the horizontal clock (-4 V).

Radiation Damage Tolerance

MPP-CCDs can tolerate more ionizing radiation damage than conventional noninverted devices. Ionization damage to the CCD manifests itself in two ways. First, when exposed to radiation new Si-SiO_2 interface states are formed as weak atomic bonds in region are broken. The new interface states translate into more hopping conduction and greater surface dark current generation. With MPP technology the new surface dark current generated is eliminated since holes induced by inversion are electronically passivated. Second, ionizing radiation creates electron-hole

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pairs within the gate oxide. These charges are mobile and become trapped at the interface causing the gate insulator to charge. This charging mechanism results in a *flat-band* shift changing the clock operating potentials of the CCD. If the flat band shift is significant the clocks may shift enough from their nominal operating range that could lead to poor CTE performance. Driving the phases deep into inversion allows the gate oxide to charge leaving the phase still pinned. For example, if inversion for a MPP-CCD occurs at -7 V and the CCD is biased and pinned at -10 V then a positive 3 V flat-band shift is allowed (oxide charging due to ionizing radiation is typically positive in nature).

For partially inverted CCDs pinning the barrier phases has the same advantage as MPP. However, the collecting phase is now vulnerable since it is not pinned. As indicated above, full well capacity is dependent on the positive level to this phase. Therefore, a shift in flat-band due to ionizing radiation will change the full well performance for the CCD. CRAF/Cassini has prepared itself for positive shifts that will occur due to the ionizing radiation environment in space. The ISS CCD cameras will therefore fly a commandable voltage for the collecting phase to off-set any flat-band shifts that occur thereby maintaining optimum full well and anti-blooming protection.

CCD Protection Diodes

It is important to mention that not all CCDs can be inverted and pinned. The main reason for this limitation is because some CCDs are "protected" with on-board *anti-electrostatic protection diodes*. For example, Thomson CSF has incorporated diodes to protect their CCDs from electrostatic discharge, diodes that limit clock drive above substrate potential (i.e., clock drive is restricted to *unipolar drive*). Clocking the Thomson CCD negatively forward biases the diodes and clamps clock drivers to about -1 V, far from the inverted state. In addition, when forward conduction occurs IR light or *luminescence* is generated by the diode (i.e., any forward biased diode will act as a LED to some degree). Luminescence is severe and saturates the CCD quickly depending on the forward bias applied. Because of the advantages inverted technology provides, Thomson will be fabricating CCDs that can be driven negatively by eliminating standard protection diodes that have limited clock drive in the past.

It has been JPL's philosophy that protection networks, such as diodes, not be employed for the following two important reasons. First, for flight CCD projects, it is critical to evaluate the reliability of the sensor in terms of high impedance shorts. Rejection criteria established long ago for shorted devices is

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that gate shorts must exhibit impedances greater than 100 Meg-ohm (characterized with 15 V applied) if they are to be considered for flight use. When protection networks are incorporated it becomes impossible to evaluate the CCD for shorts of this magnitude since the measurements are limited to the impedance of the protection devices (these impedances are typically low so that protection can be achieved). Second, it has been JPL's experience that protection networks don't under all environmental conditions protect the CCD completely. On a occasion a protected CCD is destroyed by electrostatic damage. Other damaged sensors have been found that function, however, it is difficult to assess the damage by impedance measurements for the reasons discussed above. In fact, it has been demonstrated that protected CCDs can be damaged without the user knowing about the difficulty, until its too late, because the protection networks "mask" the problem initially (i.e., *latent damage*). For example, one month before the launch of Solar-A, SXT experienced a serious problem with their flight CCD (a new column blemish appeared). Impedance measurements could not be performed on the TI VPCCD since each gate was protected with a 60 k-ohm protection resistor to substrate. The column blemish was later identified (via destructive analysis) to be related to a high impedance substrate short associated with the array transfer gate. If protection resistors were not employed the problem would have been found immediately via high impedance measurements. It is advantageous to perform regular impedance measurements at various times in the build-up and packaging of flight CCDs including an impedance test prior to when the sensor is installed into the flight camera.

10. SCIENTIFIC CCD MANUFACTURERS AND FOUNDRIES

Shown below is a current list of scientific CCD manufacturers and foundries.

Tektronix Inc.
Tektronix Industrial Park
PO Box 500, M/S 59-567
Beaverton, OR. 97077

Dr. Morley Blouke
Phone: 503-627-6064
FAX: 503-627-5560

Eastman Kodak Company
KP1-34
Rochester, NY. 14652 3708

Dr. Robert Bilhorn
Phone: 716-722-3387
FAX: 716-722-3952

David Sarnoff Research Center
CN533300, M/S SW 331A
201 Washington Road
Princeton, NJ. 08543 5300

Dr. Gary Hughes
Phone: 609-734-3056
FAX: 609-734-2225

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EG & G Reticon
345 Potrero Ave.
Sunnyvale, CA.

Dr. Hsin-Fu Tseng
Phone: 408-738-1009
FAX: 408-738-3832

English Electric Valve Ltd.
Waterhouse Lane
Chelmsford, Essex
United Kingdom CM1 2QU

Mr. John Ashton
Phone: 245-493493
FAX: 011 44 245
492492

Thomson Composants Militaries
et Spatiaux
Rue de Rocheplaine
BP 128
38521 Saint Egreve, Cedex, France

Mr. Jacuques Chautemps
Phone: 011 33 76 58 3112
FAX: 011 33 76 58 3406

Thomson Electron Tubes and Devices
40 G Commerce way
Totowa, NJ. 07511

Mr. Greg Herbison
Phone: 201-812-9000
FAX: 201-812-9050

Loral Aeronutronics Corp.
Ford Road, M/S 2-57
PO Box A
Newport Beach, CA. 92658 8900

Dr. Dick Bredthauer
Phone: 714-720-6265
FAX: 714-720-6741

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Research Laboratory), David Burrows, David Lumb, and Gordon Garmire (Pennsylvania State University), Lloyd Robinson (Lick Observatory), Alan Delamere (Ball Aerospace), Richard Griffiths (Space Telescope Institute), Bob Hlivak (Hawaii Institute of Astronomy), Andrew Holland (Leicester University), Doug Holland (NASA/Johnson Space Center), Bruce Woodgate and Jhabvala Murzy (NASA/Goddard Space Flight Center), Roger Lynds (Kitt Peak Nat'l Observatory), Bill Mc Curnin (Coherent Tucson Research Center), Nelson Saks (Naval Research Center), John Vallerga (Center for EUV Astrophysics), and John Lowrance (Princeton Scientific Instruments), and Fred Landauer (United Rope Inc.).

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12. REFERENCES

Many Scientific CCD topics examined in this paper are discussed in considerable depth in a collection of CCD publications written or co-authored by the CCD Advanced Development Group at JPL. These articles and papers can be obtained on request by telephone or letter.

Numerous articles and publications have been written by the CCD manufacturers listed in Chapter 10 providing a good source of CCD and product information.

Several CCD publications were collected and published in three CCD special issues by Optical Engineering: (1) **Charge Coupled Device Characterization, Modeling and Application**, Volume 26 Number 8, Aug. 1987, (2) **Charge Coupled Device Manufacturer and Application**, Volume 26 Number 9, Sept. 1987, (3) **Charge Coupled Device and Charge Injection Device Theory and Application**, Volume 26 Number 10, Oct. 1987.

Two general books on CCDs are: (1) **Charge-Coupled Devices and Systems**, Ed. M.J. Howes and D.V. Morgon, John Wiley and Sons, 1979. and (2) **Charge Transfer Devices**, C.H. Sequin and M.F.

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DISCUSSION

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J. Janesick: No.

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